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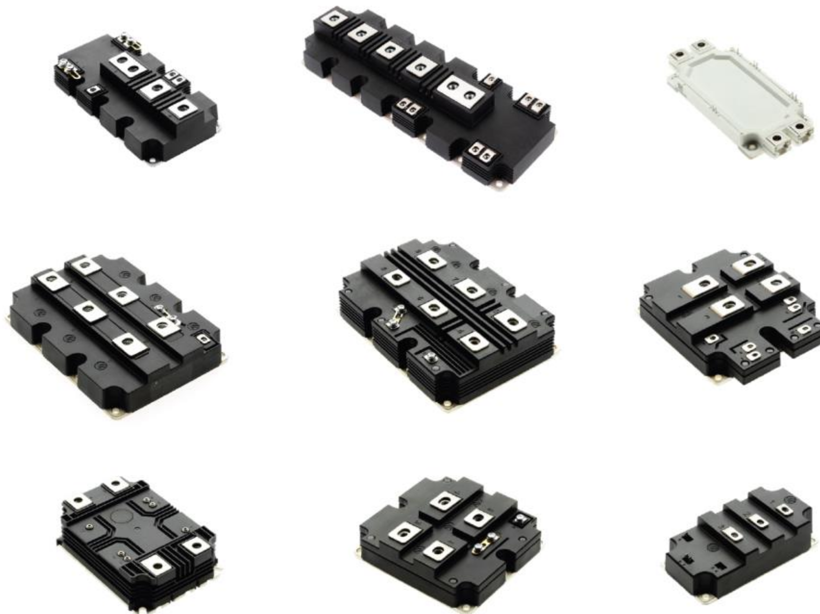
AN6440
Thermal Modelling of IGBT Modules

Application Note

AN6440-1 May 2024 LN43370



Abstract—**Overheating is identified as a primary cause of failure in semiconductor devices, leading to both immediate and progressive malfunctions. In this application note, the foundational concepts of thermal modelling for semiconductor devices with a focus on IGBT modules are explored. The application of Cauer and Foster models for the estimation of junction temperatures during both steady-state and transient operations is also discussed. This discussion is supplemented by simulation examples to provide comprehensive insights.**

1 Introduction

During operation, power semiconductor switching devices, such as IGBT modules, generate losses that result in increased temperatures across various components of the module. The IEC 60747-9 standard specifies a spectrum of temperature ratings for IGBTs, including case temperature, T_{c}, and virtual junction temperature, T_{vj} [1].

Given that IGBT modules exhibit varying power losses depending on the operating conditions of the load, it is critical to select an IGBT module that is not only appropriate for the intended load but is also paired with the cooling system to mitigate the risk of thermal runaway and early failure. Moreover, to enhance the durability of IGBT modules, it is essential to maintain minimal temperature fluctuations during operation, as significant temperature variations can induce substantial internal mechanical stress, shortening the module's operational life.

The thermal behavior of power semiconductor devices can be effectively estimated using RC thermal models, where "RC" stands for "Thermal Resistance-Capacitance". Thermal impedance, Z_{th}, combining thermal resistance, R_{th}—

Table 1. Analogy between electrical and thermal parameters.

Electrical parameter	Voltage V (V)	Current I (A)	Resistance R (Ω)	Capacitance C (F)
Thermal parameter	Temperature T (°C)	Power P (W)	Thermal resistance R_{th} (°C/W)	Thermal capacitance C_{th} (J/°C)

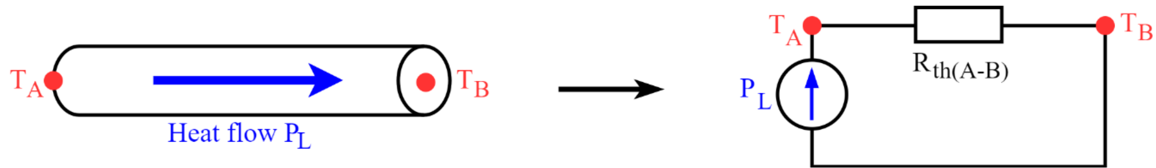


Figure 1. Thermal circuit example.

the opposition to heat flow, measured in °C/W—and thermal capacitance, C_{th}—the capacity to store thermal energy, measured in J/°C, is the key parameter for thermal modelling. These elements are fundamental for analysing both the steady-state (stationary) and transient thermal behaviours, ensuring the device's performance and reliability through effective thermal management.

These terms (Z_{th}, R_{th} and C_{th}) draw parallels with electrical circuits to conceptualise heat flow in devices. This concept of thermal-electrical analogy is encapsulated in **Table 1**. The thermal resistance and capacitance of a semiconductor device can be equivalently represented by the electrical resistance and capacitance. By considering electrical current as analogous to power and potential difference as analogous to temperature difference, any thermal circuit can be managed in a similar manner to an electrical circuit. For example, the thermal circuit presented in **Figure 1** demonstrates how to obtain the temperature difference between two specific points (such as A and B) of a device, when there is a heat flow equal P_L between those two points (assuming the thermal capacitance is negligible). According to **Table 1** and **Figure 1**, T_A can be calculated from (1) if T_B is known, where $R_{th(A-B)}$ is the thermal resistance between points A and B.

$$T_A = R_{th(A-B)} P_L + T_B \qquad (1)$$

2 Thermal impedance and resistance determination

2.1 Temperature definition

The junction temperature refers to the internal temperature of the semiconductor chip, which is critical to the device's power losses and safe operating areas. Given that the chip's temperature is not uniform, the concept of virtual junction temperature, T_{vj}, is introduced. T_{vj} can be regarded as the average temperature across the chip, based on the assumption of uniform cooling. Additionally, thermal impedance and resistance of junction to case, denoted as $Z_{th(j-c)}$ and $R_{th(j-c)}$ are specified in relation to T_{vj}, as outlined in IEC 60747-9.

For the rest of this application note, when referring to junction temperature, denoted by T_j as its symbol, it specifically addresses the concept of virtual junction temperature, T_{vj}.

The term T_{j_max} indicates the highest permissible junction temperature during the device's active state. The IGBT module baseplate temperature, known as the case temperature, T_c, may vary from T_j. Furthermore, the temperature of the heatsink, T_h, refers to the surface temperature of the heatsink to which the power module is attached. The heatsink and its cooling system are designed to efficiently manage the dissipation of heat. Through thermal analysis, it is crucial to consistently ensure that the device remains within its operational temperature limits and does not surpass its T_{j_max} during operation.

2.2 Temperature determination

T_j can be measured indirectly using a characteristic of the device that is sensitive to temperature changes, such as IGBT collector-emitter saturation voltage, V_{CE_sat}, or Diode forward voltage, V_F, at low current. Consequently, a calibration curve, for example, V_{CE_sat} as a function of T_j (i.e., $V_{CE_sat} = f(T_j)$), need to be established so that it can be later used for T_j measurement. This calibration involves recording the curve while applying uniform and homogeneous external heating to the power device until thermal equilibrium is achieved at each measurement point. The current through the device during measurement should be maintained at a very low level to ensure internal heat generation is insignificant. This indirect T_j measurement can be considered T_{vj}.

An exemplar calibration curve used to determine T_j by measuring the saturation voltage at a defined measuring current is presented in **Figure 2**. It should be mentioned that at very low current levels, IGBTs usually display a negative temperature coefficient for V_{CE_sat} and therefore V_{CE_sat} reduces with the increase of T_j.

T_c and T_h are usually measured using thermocouples. These thermocouples are designed to be thermally isolated along their length, with the exception of their upper ends. It is at these points that they make direct contact with the module's baseplate and the heatsink. For precise measurement, the axis of each thermocouple should be strategically positioned at the center of each chip.

2.3 Thermal impedance measurement procedure

The methodology for measuring thermal impedance, as outlined in IEC 60747-9, is presented in **Figure 3**. This process involves applying a constant power, P_{device}, to the IGBT module by inducing a current flow that leads to a stable T_j after an initial transient phase. Once the power is switched off, the module's cooling process is monitored and T_j, T_c and T_h are measured using the methods presented in section 2.2.

Thermal resistance, denoted as $R_{th(x-y)}$ (where 'x' and 'y' can represent 'j' for junction, 'c' for case, and 'h' for heatsink) is calculated by taking

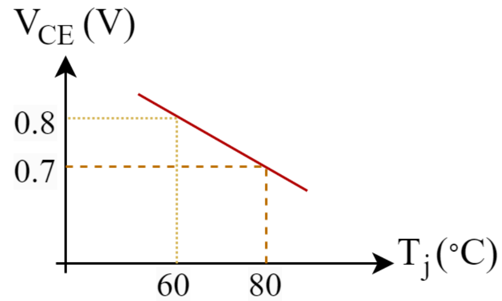


Figure 2. Exemplar calibration curve measured at a low constant current with the external heating (when heated from outside, $T_j = T_c$).

the temperature difference at time equals zero (difference of $T_x(t=0)$ and $T_y(t=0)$) and dividing it by P_{device} as presented by (2). To compute the time-dependent thermal impedance, $Z_{th(x-y)}(t)$, the recorded temperature trajectories are reflected vertically and repositioned to the coordinate system's origin. Subsequently, $Z_{th(x-y)}(t)$ is determined by dividing the temperature difference between $T_x(t)$ and $T_y(t)$ at any given time by P_{device} as presented by (3).

$$R_{th(x-y)} = \frac{T_x(t=0) - T_y(t=0)}{P_{device}} \quad (2)$$

$$Z_{th(x-y)}(t) = \frac{T_x(t) - T_y(t)}{P_{device}} \quad (3)$$

The efficiency of the cooling path from the junction to the ambient environment significantly influences the thermal impedance of the power module. Water-cooled heatsinks are known for their effective cooling capabilities that minimises heat spreading and leads to more efficient heat dissipation. In contrast, air-cooled heatsinks, which are generally less efficient, result in greater heat distribution to neighbouring components. The thermal impedance of the power module is typically increased with more efficient cooling methods that effectively limit heat spreading. Therefore, when measuring the module Z_{th} and R_{th}, efficient water-cooled heatsinks should be used to resemble the worst-case scenario. Additionally, the thermal resistance of the thermal interface material (TIM) plays a vital role in influencing the module's thermal impedance. Consequently, it is essential to aim for the highest quality in the TIM

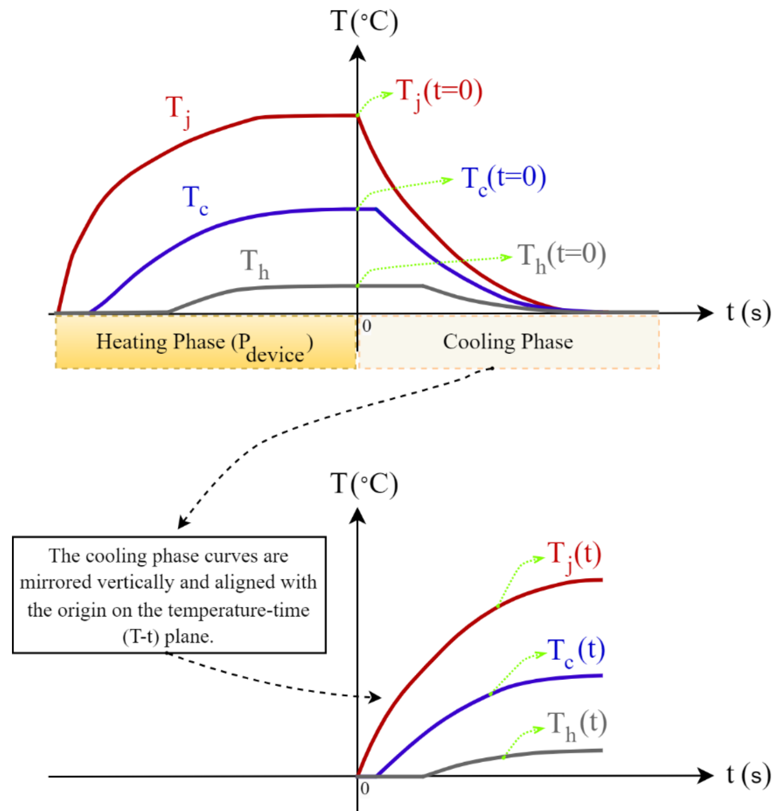


Figure 3. Methodology of thermal impedance measurement.

layer. For detailed instructions on the correct mounting of an IGBT module, please refer to Dynex application note AN4505 [2].

3 Thermal equivalent circuit models

The method for calculating the steady-state T_j of IGBT and Diode, given the known power losses of the IGBT chips and diode chips (where diodes are present), is straightforward when using a one-dimensional thermal circuit, as presented in **Figure 4**. This thermal circuit enables easy electrical analysis (as detailed in section 1) or simulation to determine the steady-state T_j for both the IGBT and diode. In this thermal circuit, the thermal resistances for the IGBT ($R_{\mathrm{th(j-c)_IGBT}}$), diode ($R_{\mathrm{th(j-c)_diode}}$), from the case to heatsink ($R_{\mathrm{th(c-h)}}$), and from the heatsink to ambient ($R_{\mathrm{th(h-a)}}$) can be sourced from datasheets. Further details on this calculation method are available in the Dynex application note AN6156 [3].

In certain cases, the transient thermal response of the IGBT module is just as crucial as its steady-state performance. Under these conditions, thermal capacitors should not be regarded as open circuits; instead, they must be incorporated into the thermal circuit analysis. To accurately investigate the thermal dynamics of semiconductor components in both transient and steady-state operations, various equivalent circuit models have been developed. Among these, the Cauer and Foster models are particularly notable. These models offer a comprehensive view of semiconductor thermal behavior under both transient and steady-state conditions and are thoroughly examined in this section.

3.1 Cauer model

The Cauer model, as shown in **Figure 5**, accurately represents the physical configuration of the module by including thermal capacitances and thermal resistances of each layer. This model is particularly effective when the properties of each layer within the module are known, allowing for the calculation or simulation of the

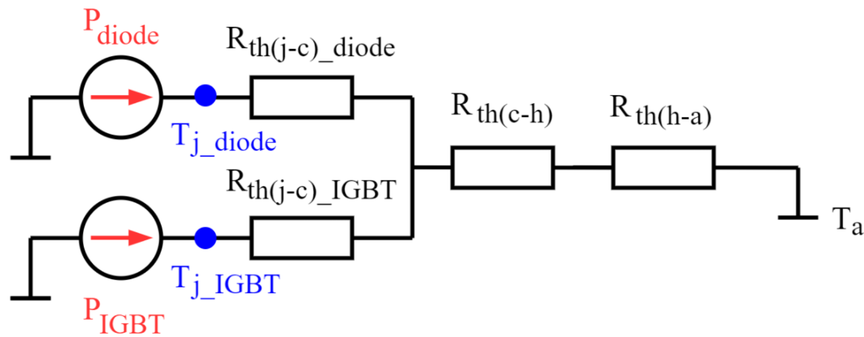


Figure 4. Thermal circuit for steady-state junction temperature estimation using one-dimensional thermal circuit. T_a is the ambient temperature.

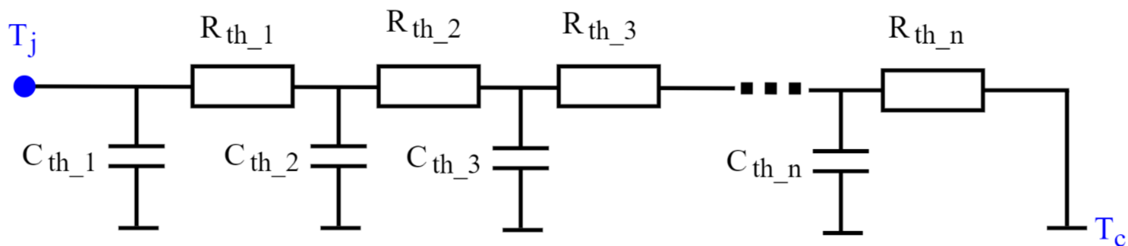


Figure 5. Cauer model. The RC elements are assigned to the package layers and represent the physical property and packaging structure of the module.

thermal resistance and capacitance of each layer. However, accurately representing how heat spreads across these layers remains a challenge and thicker layers might need to be divided into several RC elements (thermal resistor, $R_{\text{th_i}}$, and thermal capacitor, $C_{\text{th_i}}$).

The Cauer model organises the module structure into distinct n layers—such as the chip, chip solder, substrate, substrate solder, and base plate—each associated with specific RC elements. Therefore, this arrangement facilitates monitoring the internal temperatures throughout the different layers of the semiconductor, providing detailed insights into its thermal behavior.

3.2 Foster model

Creating an accurate Cauer model tends to be challenging due to the necessity of precisely understanding the internal geometry, materials, and effective heat pathways within the device. Cauer model also often requires the use of finite element method (FEM) for accurate determination of RC elements. Conversely, the Foster model, shown in **Figure 6**, has wider popularity for its simpler approach. It derives its RC elements from the thermal impedance of the devices through mathematical calculation. Therefore, this model does not rely on detailed knowledge of the device's internal structure or material composition, making it more accessible and practical choice.

IGBT module datasheets commonly present thermal impedance characteristics, Z_{th}. For example, in **Figure 7**, the Z_{th} curve of Dynex module DIM1000ASM65-UF000 is shown. In the Foster model, the RC elements are chosen to match the numerical Z_{th} characteristics, as presented in (4). The values of the RC elements in the Foster model do not directly correspond to the physical layers of the module and they basically have no physical meaning.

As presented in (4), the thermal impedance's analytical expression can be defined using the variables $R_{\text{th_i}}$ and $\tau_{\text{th_i}}$, where $\tau_{\text{th_i}}$ is the product of $R_{\text{th_i}}$ and $C_{\text{th_i}}$ ($\tau_{\text{th_i}} = R_{\text{th_i}} \times C_{\text{th_i}}$). The specific number, n, of RC (resistor-capacitor) terms in the Foster model is not critical; the primary goal is for the model to accurately align with measured Z_{th} data.

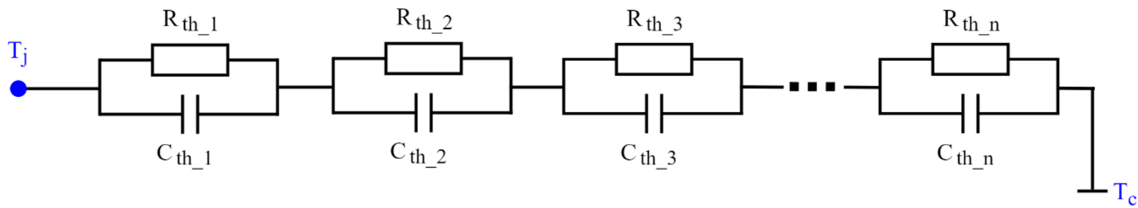


Figure 6. Foster model. The RC elements are curve-fitting parameters and do not represent the physical property and packaging structure of the module.

$$Z_{\text{th(j-c)}}(t) = \sum_{i}^{n} R_{\text{th_i}}(1 - e^{\frac{-t}{\tau_{\text{th_i}}}}) \quad (4)$$

The Foster model simplifies the representation of thermal impedance, focusing on achieving a good fit with practical Z_{th} data rather than detailing the physical properties of the system. Therefore, this model lacks the detailed insights that the Cauer model offers, and it performs well only when the temperature of the device's case remains constant, a condition that may not always be met in practical applications.

3.3 Thermal modelling of the connected module and heatsink

In practical applications, a power module is typically mounted on a heatsink using an interface material, like thermal grease, to ensure optimal thermal contact. This setup results in the thermal impedance of the interface material and the heatsink being connected in series with the thermal impedance of the module itself. The question that arises is: which model, Cauer or Foster, performs better when connected to external thermal resistors/capacitors?

3.3.1 Thermal model of a system: Cauer model

A straightforward approach is the series connection of the Cauer model of the module, the thermal resistance, $R_{\text{th_TIM}}$, and capacitance, $C_{\text{th_TIM}}$, of the TIM and the thermal resistance, $R_{\text{th_h}}$, and capacitance, $C_{\text{th_h}}$, of the heatsink.

The Cauer model, along with the integration of similar individual models of TIM and heatsink, effectively shows the physical principle where individual layers sequentially transfer heat to each other. In this framework, heat flow, represented as the current in the model from **Figure 8**, travels to the heatsink, introducing a measurable delay before the heatsink absorbs the heat. This gradual process can be accurately modeled through simulations or calculation. This method provides a detailed understanding of how heat propagates through the system, allowing for a precise analysis of thermal dynamics within layered structures. It's worth noting that accurately representing the heatsink's thermal model may require the inclusion of multiple RC branches.

Even though this method provides results with a good accuracy, the problem is datasheets usually do not provide Cauer model and it needs a detailed thermal analysis of the entire setup using FEM for the specific operating condition.

3.3.2 Thermal model of a system: Foster model

An alternative strategy involves creating a series connection using the Foster model of the module using the data specified in its datasheet,

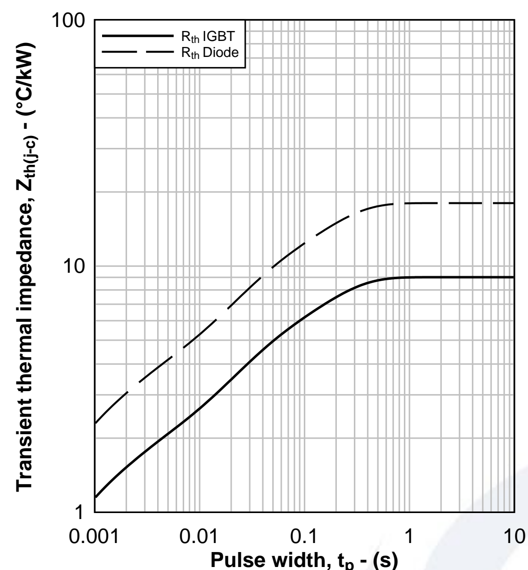


Figure 7. Transient thermal impedance of DIM1000ASM65-UF000.

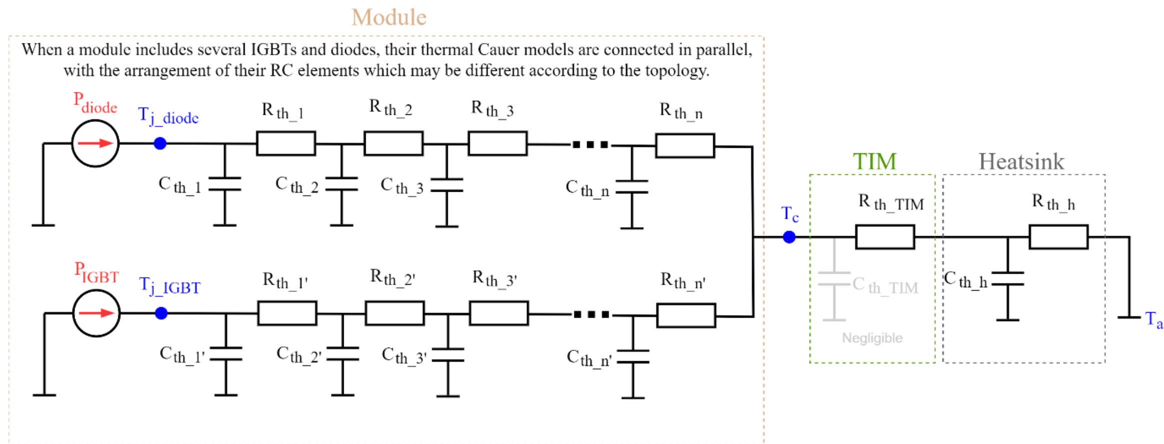


Figure 8. Series connection of the entire thermal system using Cauer model. Complicated heatsinks may require multiple RC branches.

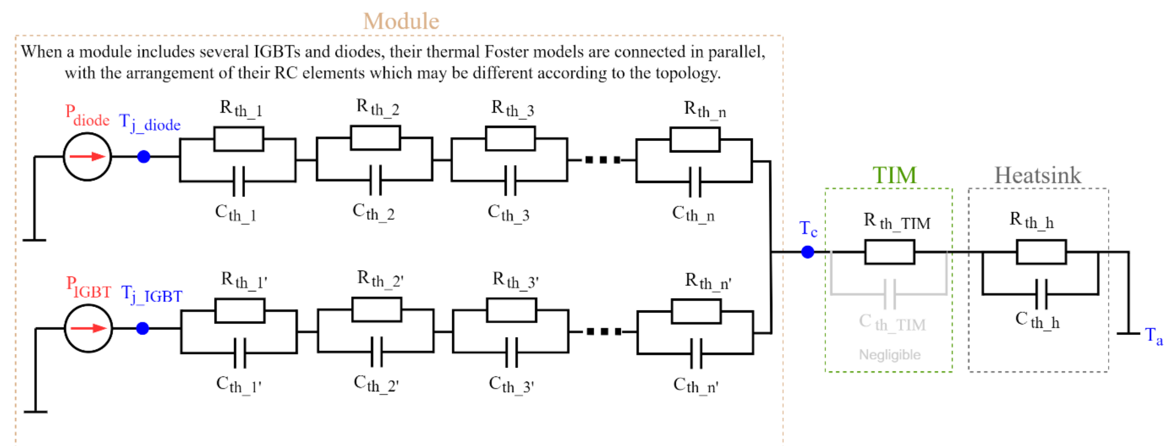


Figure 9. Series connection of the entire thermal system using Foster model. Complicated heatsinks may require multiple RC branches.

and connecting it in series with Foster models of the TIM and the heatsink. This method, which is shown in **Figure 9**, does not need any detailed FEM and can easily be used to estimate T_j. However, this method of linking Foster models in series is prone to yielding less accurate outcomes, particularly in the transient response.

When employing the Foster model, at the beginning of the current conduction, the generated heat is transmitted directly through the heat capacitors (capacitors behave basically like a short-circuit at the beginning of the transient) to the thermal resistance of the TIM, resulting in an instantaneous temperature increase in the case. This immediate change also leads to a step response in T_j, showing a direct and rapid effect of heat flow on the thermal characteristics of the system. As a consequence, in the Foster model, T_c and T_j can be too high at the beginning of the transient period. This discrepancy (error) becomes even more severe in the case of heatsinks with low time constants (such as those that are water-cooled).

When power loss (generated heat) varies over time, the capacitors in the Foster model are unable to effectively transfer the heat to the case with delay (as would be expected in practical scenarios). In other words, in a Foster model, thermal resistances and capacitances are connected in parallel, implying that heat flows simultaneously through all paths, which does not accurately reflect the physical propagation of heat through the material layers. Consequently, generated heat is directly transferred to the thermal resistance of the TIM during each transient,

resulting in significant oscillations. Therefore, the simplification involved in the series connection of Foster models can introduce significant errors.

On the other hand, when the T_c can be assumed constant (for instance, when the load duration is negligibly short compared to the time constants of the heatsink) and for a stationary operating result, the Foster model can be sufficiently accurate. In addition, if an IGBT setup is implemented and its power losses, $P_{\mathrm{device}}(t)$, are known, calculating the T_j becomes possible through direct measurement of the case temperature, $T_c(t)$. In other words, once the T_c is known, it can be effectively utilised in the Foster model to calculate T_j with a better accuracy and the thermal modelling of the TIM and heatsink is not needed anymore.

By measuring the thermal impedance with the entire assembly, including the module, TIM, and heatsink, the thermal impedances of the TIM and heatsink are integrated into the module's overall thermal impedance. As a result, in the Foster thermal model obtained from this thermal impedance, there is no small capacitance at the end of the chain (see **Figure 9**), preventing an immediate increase in the junction temperature. This method is the most accurate, but it necessitates setting up the complete system and conducting thermal impedance measurements as detailed in section 2.3.

It should be noted that if the datasheet specifies the thermal resistance from case to heatsink separately for the IGBT and diode, $R_{\mathrm{th_TIM}}$ should be calculated as their parallel equivalent.

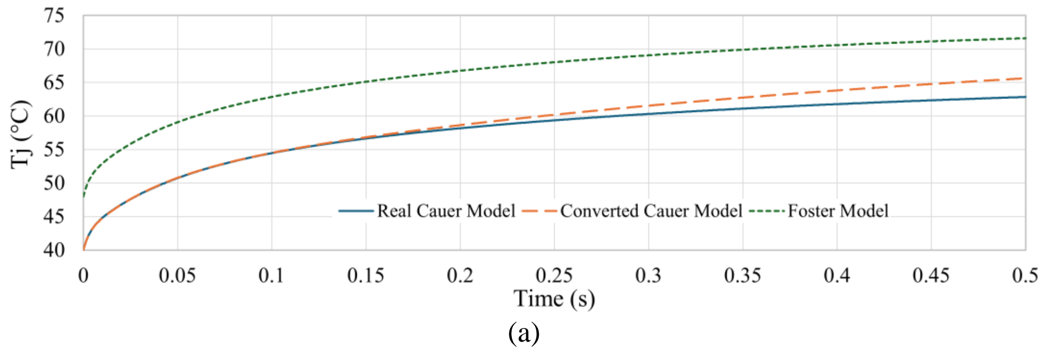
3.3.3 Thermal model of a system: Transforming the Foster model to the Cauer model

The Foster model can be converted to a Cauer model through mathematical transformation, as outlined in [4], and the new model can be again used in **Figure 8**. Converting the characteristics outlined in the datasheet (such as thermal diagrams or the Foster model data) to a Cauer Model is feasible, but it is not a one-to-one transformation and may result in varying $R_{\mathrm{th_i}}$ and $C_{\mathrm{th_i}}$ values for identical $Z_{\mathrm{th(j-c)}}$ characteristics. In other words, this conversion process does not accurately reflect the physical layering, and particularly, the total thermal capacitance of the transformed model can significantly differ—by orders of magnitude—from the actual effective heat capacity of the power module. Therefore, when such a model is integrated with a heatsink, the resulting thermal impedance from junction to ambient ($Z_{\mathrm{th(j-a)}}$) of the combined system could be considerably inaccurate. However, this approach benefits from the structure of the Cauer model, resulting in enhanced accuracy for estimating the junction temperature during transient operations.

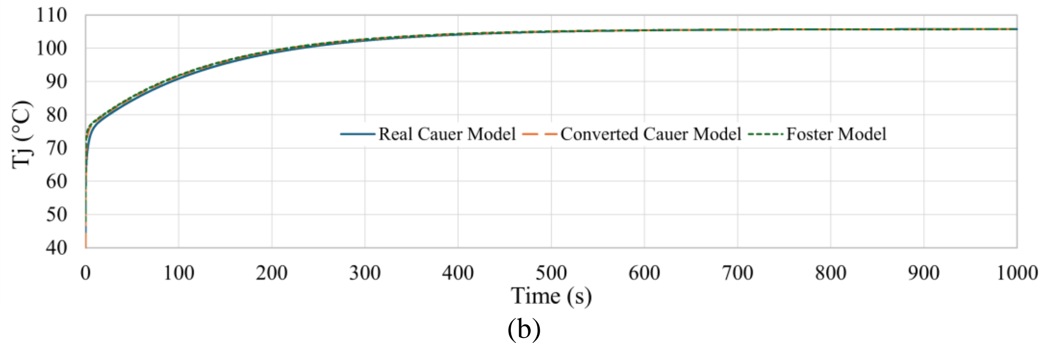
3.3.4 Thermal model of a system: Simulation

To validate the claims made regarding the Foster model and the transformed Cauer model, this section offers a comparative analysis. Firstly, the real Cauer model of an IGBT module is derived from knowledge of structure. Secondly, by simulating the real Cauer model in PLECS and utilising the thermal circuit presented in **Figure 5** and (4), the thermal impedance and the Foster model of the IGBT module are obtained. Following this, the Foster model can be transformed into a Cauer model through mathematical transformation, as outlined in [4] (PLECS can also be used to transform the Foster model into a Cauer model). As the three models have identical thermal impedance curve, this process enables a comparison between the Foster model and the converted Cauer model, with the real Cauer model serving as the benchmark.

When there is a constant power loss in the IGBT, the junction temperatures derived from the three models are obtained through simulation in PLECS and presented in **Figure 10**. Initially, during the transient period, the Foster model exhibits a significant discrepancy when compared to the real Cauer model.
Additionally, the converted Cauer model also shows some discrepancies, indicating it does not possess the same thermal capacitance as the real Cauer model, despite both models sharing identical thermal impedance curve. Nevertheless, both the Foster and Cauer models achieve a good level of agreement with the real Cauer model in the steady-state.

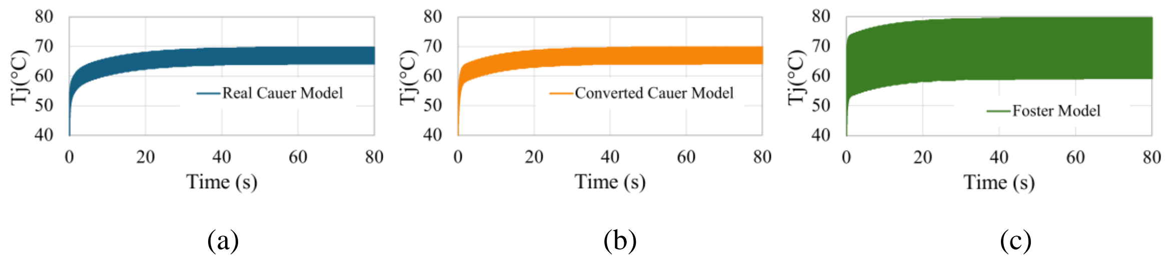


(a)



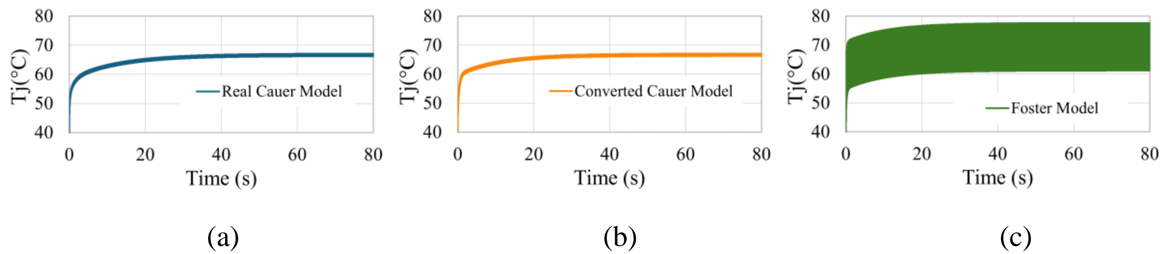
(b)

Figure 10. Real Cauer, converted Cauer and Foster model comparison under constant power loss. (a) For transient. (b) For steady-state.



(a) (b) (c)

Figure 11. Junction temperature comparison of (a) the real Cauer model, (b) the converted Cauer model, and (c) the Foster model under variable power loss at a frequency of 50 Hz.



(a) (b) (c)

Figure 12. Junction temperature comparison of (a) the real Cauer model, (b) the converted Cauer model, and (c) the Foster model under variable power loss at a frequency of 500 Hz.

The comparison becomes more interesting when the power loss is not constant over time, reflecting a more realistic scenario. T_j calculated using the three models, when the power loss follows a half-rectified sine wave shape, are presented in **Figure 11** and **Figure 12** for frequencies of 50 Hz and 500 Hz, respectively. Once again, the Foster model leads to greater oscillation, as the configuration of capacitors in parallel with resistors fails to effectively filter and suppress these high frequency oscillations.

4 Final remarks

The most reliable thermal impedance of a system (junction to ambient, $Z_{\mathrm{th(j-a)}}$) can be achieved by a direct measurement, as outlined in section 2.3, of the full setup including the module, TIM and heatsink. Later an analytical Foster model can be fitted to this measurement. Therefore, this method delivers a Foster model of the entire system, with which the junction temperature can be calculated fault-free.

When direct measurement of the entire system is impractical, and there is a need to integrate module and heatsink models, the uncertainty—particularly in transient scenarios—significantly increases. Under these circumstances, it's advisable to introduce reasonable margins. The most effective approach in such instances is to employ series-connected Cauer models, following their transformation from the Foster model. However, it is essential to ensure that the Cauer models accurately reflect the module's physical properties, especially concerning total heat capacity.

If the Foster models of a system must be connected together for any reason, the limitations and possible significant errors of this approach should be considered. However, when the case temperature can be assumed constant (for example, when the load duration is negligibly short compared to the heatsink's thermal time constant), the junction temperature during the short transient can be accurately calculated by only considering the thermal impedance of the module and neglecting the rest. Additionally, for stationary operating conditions, the Foster model can provide sufficient accuracy.

5 References

[1] International Standard IEC 60747: Semiconductor devices – Discrete devices – Part 9: IGBTs, Edition 2.0, 2007.

[2] High Voltage IGBT Thermal Budgeting and Module Mounting Guidance, AN4505, Dynex Semiconductor Ltd.

[3] Calculating Power Losses in an IGBT Module, AN6156, Dynex Semiconductor Ltd.

[4] Y. C. Gerstenmaier,W. Kiffe, and G.Wachutka, “Combination of thermal subsystems modeled by rapid circuit transformation,” in Proc. Therminic, 2007, pp. 115–120.

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