

FEATURES

- Double Side Cooling
- High Surge Capability
- Very Low Cosmic Ray FIT Rating
- High dV/dt Rating

APPLICATIONS

- Multi-level VSC Bypass thyristor for HVDC

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
ACR2900VR45	1000 / 4500	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 400\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

ACR2900VR45

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	1000V
V_{DRM}	4500V
$I_{T(AV)}$	2900A
I_{TSM}	39000A
dV/dt	10kV/μs
dI/dt	400A/μs

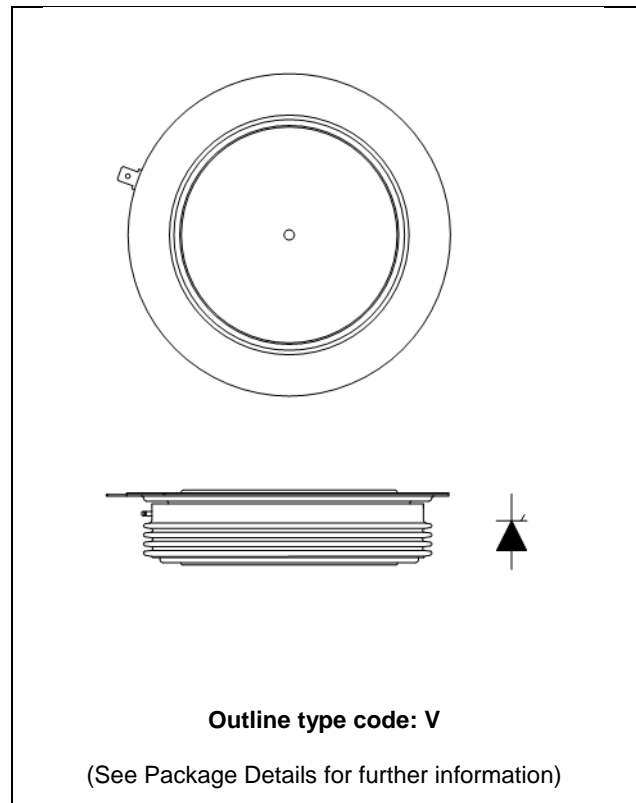


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}C$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2900	A
$I_{T(RMS)}$	RMS value	-	4555	A
I_r	Continuous (direct) on-state current	-	4420	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}C$	39	kA
I^2t	I^2t for fusing	$V_R = 0$	7.6	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	0.00746	$^{\circ}C/W$
		Single side cooled	Anode DC	-	0.0130	$^{\circ}C/W$
			Cathode DC	-	0.0178	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	0.002	$^{\circ}C/W$
			Single side	-	0.004	$^{\circ}C/W$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	$^{\circ}C$
T_{stg}	Storage temperature range			-55	125	$^{\circ}C$
F_m	Clamping force			48	59	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C		-	400	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 60°C, gate open		-	10000	V/μs
dI/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)} Gate source 30V, 10Ω tr < 0.5μs, T _j = 125°C	Non-repetitive	-	400	A/μs
V_{T(RO)}	Threshold voltage - Low level	300A to 2600A at T _{case} = 125°C		-	0.82	V
	Threshold voltage - High level	2600A to 8000A at T _{case} = 125°C		-	1.08	V
r_T	On-state slope resistance - low level	300A to 2600A at T _{case} = 125°C		-	0.30	mΩ
	On-state slope resistance - High level	2600A to 8000A at T _{case} = 125°C		-	0.20	mΩ
t_{gd}	Delay time	V _D = 67% V _{DRM} , I _g = 3A tr = 0.5μs, T _j = 25°C, tp = 40μs		-	3	μs
V_{pu}	Pick-up Voltage	I _g = 3A, tr = 0.5μs, T _j = 25°C, tp = 40μs		-	2	V
I_L	Latching current	T _j = 25°C, V _D = 5V		-	3	A
I_H	Holding current	T _j = 25°C, R _{G-K} = ∞, I _{TM} = 500A, I _T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25°C	350	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	15	mA

CURVES

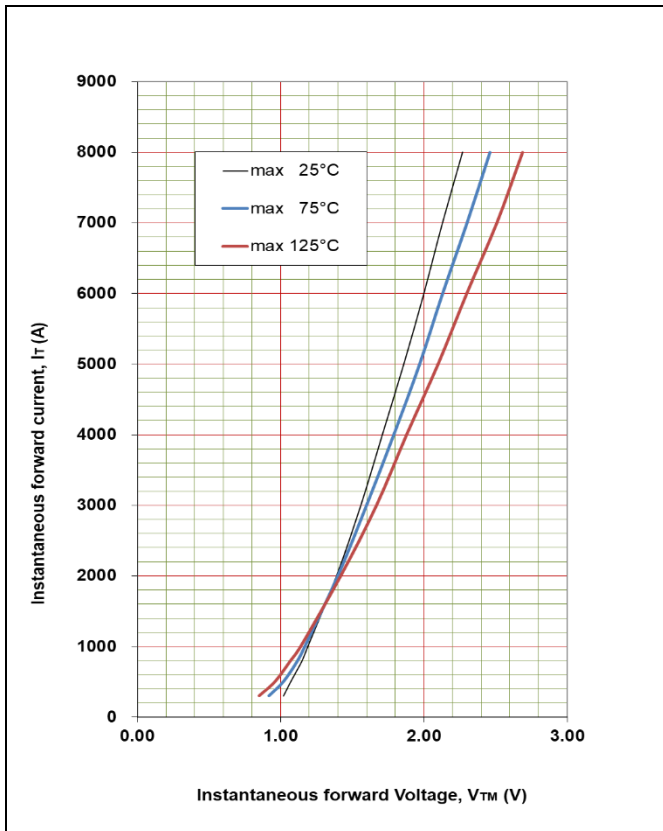


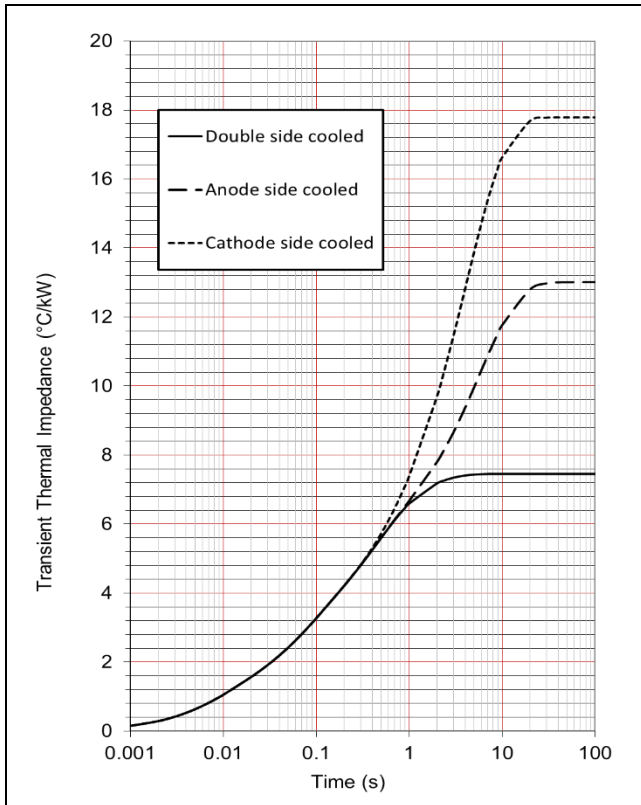
Fig. 2 Maximum on state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.035542
 B = 0.131586
 C = 0.000179
 D = 0.000591

These values are valid for T_j = 125°C for I_T 300A to 8000A



		1	2	3	4
Double side cooled	Ri(°C/kW)	0.9206	1.8299	3.4022	1.3044
	Ti(s)	0.007681	0.05795	0.4079	1.2085
Anode side cooled	Ri(°C/kW)	0.9032	1.6719	3.0101	7.4269
	Ti(s)	0.007587	0.05365	0.3145	5.6240
Cathode side cooled	Ri(°C/kW)	0.9478	2.0661	1.6884	13.0847
	Ti(s)	0.007844	0.06455	0.3894	4.1447

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

ΔR_{th(j-c)} Conduction

Tables show the increments of thermal resistance R_{th(j-c)} when the device operates at conduction angles other than d.c.

Double side cooling		
θ°	ΔZ _{th} (z)	
	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.83	1.54
60	2.08	1.81
30	2.27	2.11
15	2.36	2.28

Anode Side Cooling		
θ°	ΔZ _{th} (z)	
	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.84	1.54
60	2.08	1.81
30	2.28	2.11
15	2.37	2.28

Cathode Sided Cooling		
θ°	ΔZ _{th} (z)	
	sine.	rect.
180	1.33	0.88
120	1.57	1.29
90	1.83	1.53
60	2.07	1.80
30	2.26	2.10
15	2.35	2.26

Fig. 3 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

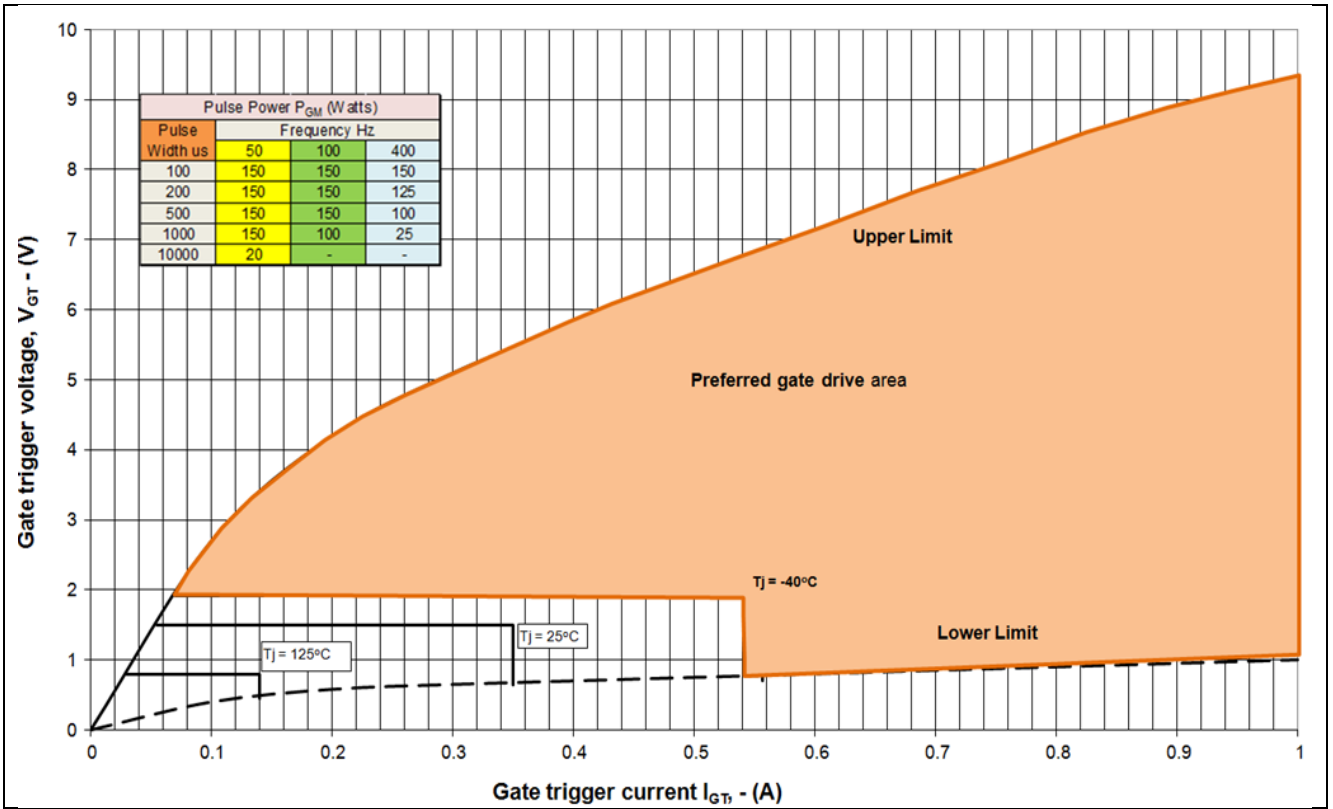


Fig. 4 Gate characteristics

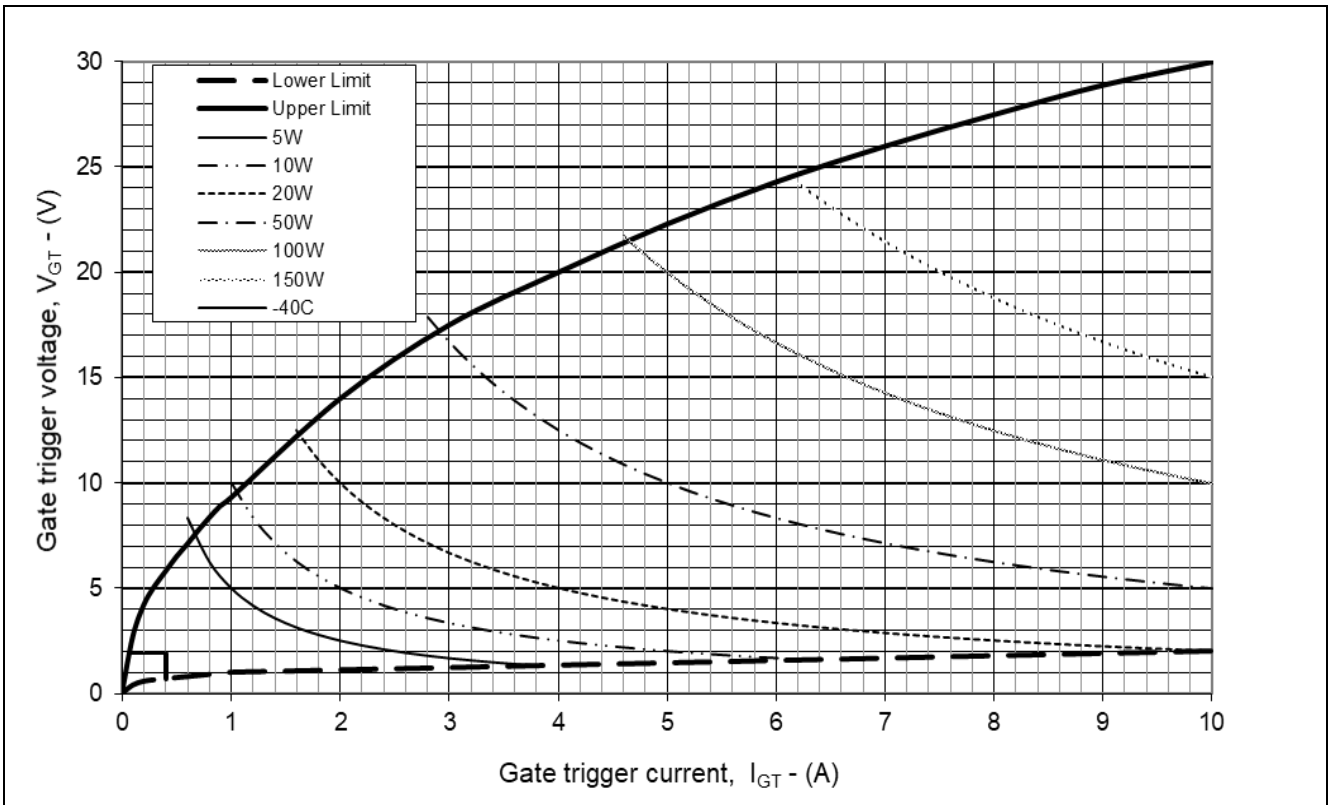


Fig. 5 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

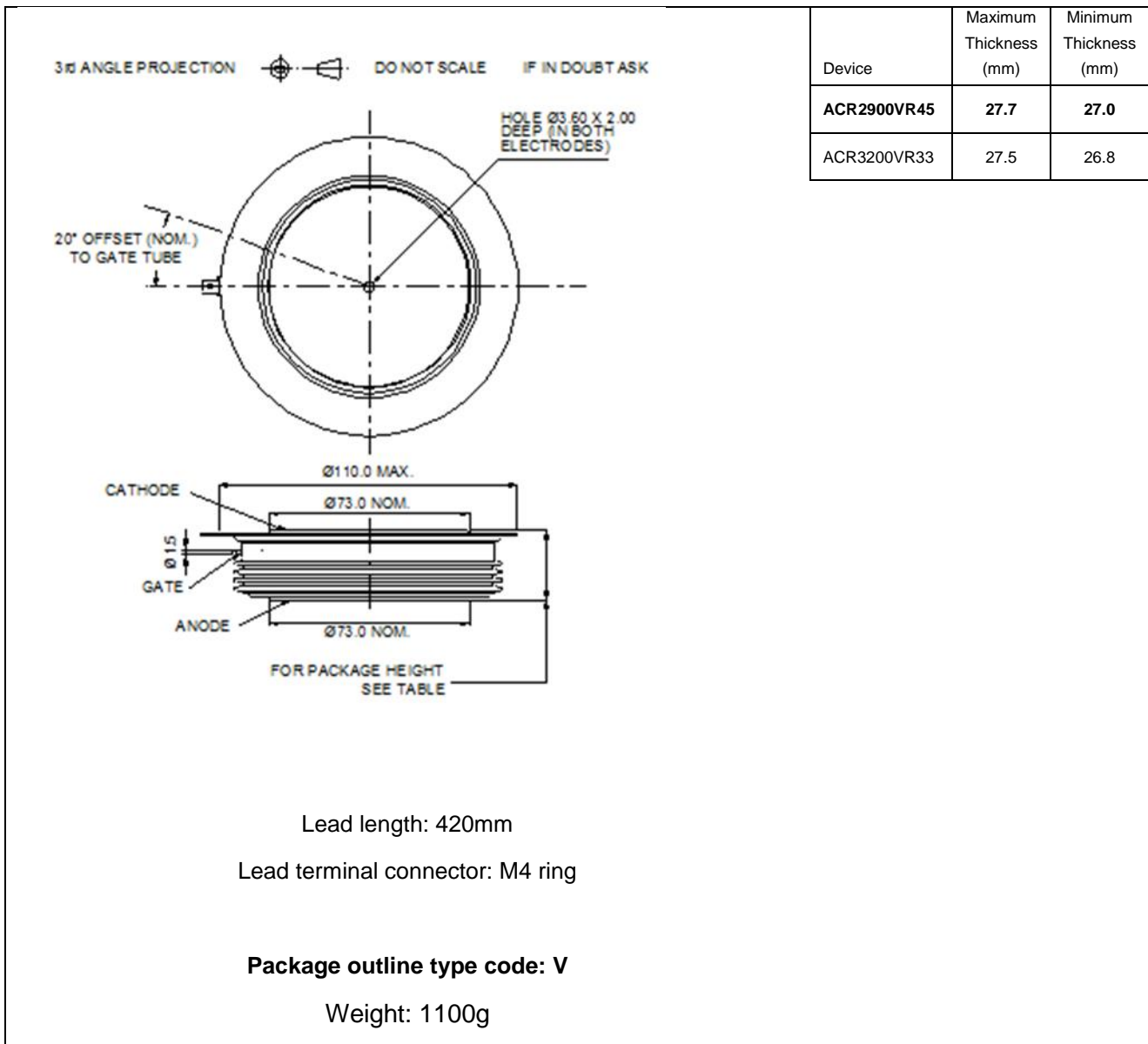


Fig. 6 Package outline

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Target Information:	This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.
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