# DCR1840Y85

## Phase Control Thyristor

Replaces DS5767-3 DS5767-4 March 2023 (LN42480)

## FEATURES

- Double Side Cooling
- High Surge Capability

## APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

## KEY PARAMETERS

| | |
|---|---|
| $V_{DRM}$ | **8500V** |
| $I_{T(AV)}$ | **1830A** |
| $I_{TSM}$ | **25000A** |
| **dV/dt*** | **1500V/µs** |
| **dI/dt** | **300A/µs** |

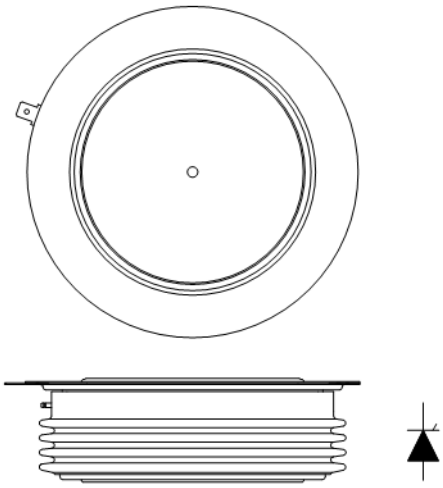
*** Higher dV/dt selections are available on request**

## VOLTAGE RATINGS

| Part and Ordering Number | Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ (V) | Conditions |
|---|---|---|
| DCR1840Y85*<br>DCR1840Y80<br>DCR1840Y75<br>DCR1840Y70 | 8500<br>8000<br>7500<br>7000 | $T_{vj}$ = -40°C to 125°C, $I_{DRM}$ = $I_{RRM}$ = 300mA, $V_{DRM}$, $V_{RRM}$ $t_p$ = 10ms $V_{DSM}$ & $V_{RSM}$ = $V_{DRM}$ & $V_{RRM}$ + 100V respectively |

Lower voltage grades available.

*8200V @ -40°C, 8500V @ 0°C



**Outline type code: Y**

(See Package Details for further information)

**Fig. 1 Package outline**

## ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

**DCR1840Y85**

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

## CURRENT RATINGS

**$T_{case}$ = 60°C unless stated otherwise**

| Symbol | Parameter | Test Conditions | Max. | Units |
|---|---|---|---|---|
| **Double Side Cooled** | | | | |
| $I_{T(AV)}$ | Mean on-state current | Half wave resistive load | 1830 | A |
| $I_{T(RMS)}$ | RMS value | - | 2870 | A |
| $I_T$ | Continuous (direct) on-state current | - | 2750 | A |

## SURGE RATINGS

| Symbol | Parameter | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $I_{TSM}$ | Surge (non-repetitive) on-state current | 10ms half sine, $T_{case}$ = 125°C<br>$V_R$ = 0 | 25.0 | kA |
| $I^2t$ | $I^2t$ for fusing | | 3.13 | $MA^2s$ |

## THERMAL AND MECHANICAL RATINGS

| Symbol | Parameter | Test Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{th(j-c)}$ | Thermal resistance - junction to case | Double side cooled | DC | - | 8.4 | °C/kW |
| | | Single side cooled | Anode DC | - | 13.4 | °C/kW |
| | | | Cathode DC | - | 23.1 | °C/kW |
| $R_{th(c-h)}$ | Thermal resistance - case to heatsink | Clamping force 54kN (with mounting compound) | Double side | - | 2.0 | °C/kW |
| | | | Single side | - | 4.0 | °C/kW |
| $T_{vj}$ | Virtual junction temperature | Blocking $V_{DRM}$ / $V_{RRM}$ | | - | 125 | °C |
| $T_{stg}$ | Storage temperature range | | | -55 | 125 | °C |
| $F_m$ | Clamping force | | | 48 | 59 | kN |

## DYNAMIC CHARACTERISTICS

| Symbol | Parameter | Test Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{RRM}/I_{DRM}$ | Peak reverse and off-state current | At $V_{RRM}/V_{DRM}$, $T_{case}$ = 125°C | | - | 300 | mA |
| $V_{TM}$ | Instantaneous forward voltage | At 4000A peak, $T_j$ = 125°C | | 3.10 | 3.50 | V |
| dV/dt | Max. linear rate of rise of off-state voltage | To 67% $V_{DRM}$, $T_j$ = 125°C, gate open | | - | 1500 | V/µs |
| dI/dt | Rate of rise of on-state current | From 67% $V_{DRM}$ to 2x $I_{T(AV)}$<br>Gate source 30V, 10Ω<br>$t_r$ < 0.5µs, $T_j$ = 125°C | Repetitive 50Hz | - | 150 | A/µs |
| | | | Non-repetitive | - | 300 | A/µs |
| $V_{T(TO)}$ | Threshold voltage - Low level | 500A to 1500A at $T_{case}$ = 125°C | | - | 1.04 | V |
| | Threshold voltage - High level | 1500A to 7000A at $T_{case}$ = 125°C | | - | 1.29 | V |
| $r_T$ | On-state slope resistance - low level | 500A to 1500A at $T_{case}$ = 125°C | | - | 0.72 | mΩ |
| | On-state slope resistance - High level | 1500A to 7000A at $T_{case}$ = 125°C | | - | 0.55 | mΩ |
| $t_{gd}$ | Delay time | $V_D$ = 67% $V_{DRM}$, gate source 30V, 10Ω<br>$t_r$ = 0.5µs, $T_j$ = 25°C | | - | 3 | µs |
| $t_q$ | Turn-off time | $T_j$ = 125°C, $V_R$ = 200V, dI/dt = 1A/µs,<br>$dV_{DR}/dt$ = 20V/µs linear | | - | 1200 | µs |
| $Q_S$ | Stored charge | $I_T$ = 2000A, $T_j$ = 125°C, dI/dt = 1A/µs<br>$V_{R(peak)}$ ~ 5100V, $V_{RM}$ ~ 3400V | | 4920 | 7040 | µC |
| $I_{RR}$ | Reverse recovery current | | | 51 | 63 | A |
| $I_L$ | Latching current | $T_j$ = 25°C, $V_D$ = 5V | | - | 3 | A |
| $I_H$ | Holding current | $T_j$ = 25°C, $R_{G-K}$ = ∞, $I_{TM}$ = 500A, $I_T$ = 5A | | - | 300 | mA |

## GATE TRIGGER CHARACTERISTICS AND RATINGS

| Symbol | Parameter | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $V_{GT}$ | Gate trigger voltage | $V_{DRM}$ = 5V, $T_{case}$ = 25°C | 1.5 | V |
| $V_{GD}$ | Gate non-trigger voltage | At 50% $V_{DRM}$, $T_{case}$ = 125°C | 0.4 | V |
| $I_{GT}$ | Gate trigger current | $V_{DRM}$ = 5V, $T_{case}$ = 25°C | 400 | mA |
| $I_{GD}$ | Gate non-trigger current | At 50% $V_{DRM}$, $T_{case}$ = 125°C | 15 | mA |

## CURVES

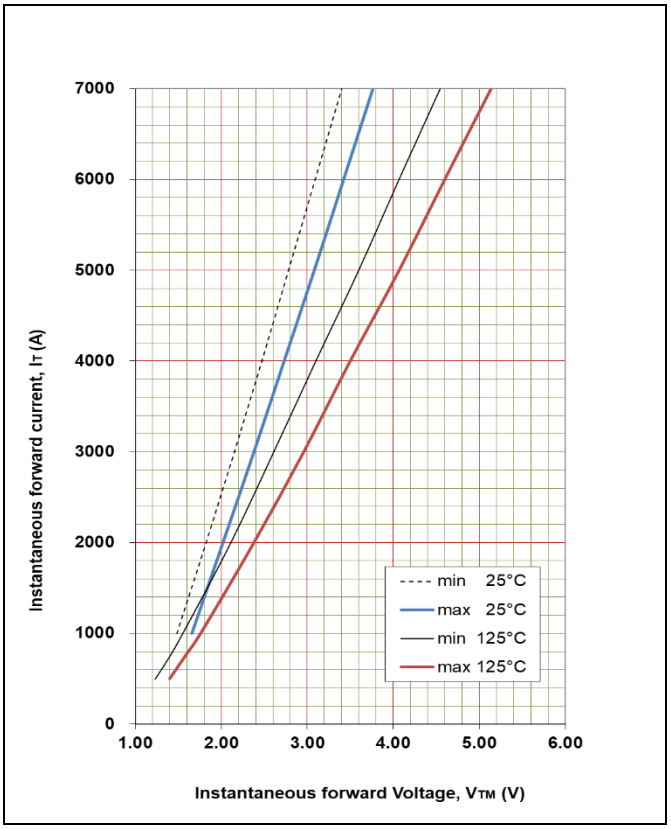



**Fig. 2 Maximum & minimum on state characteristics**

## $V_{TM}$ EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.525462
B = 0.077304
C = 0.000479
D = 0.006921

These values are valid for $T_j$ = 125°C for $I_T$ 500A to 7000A

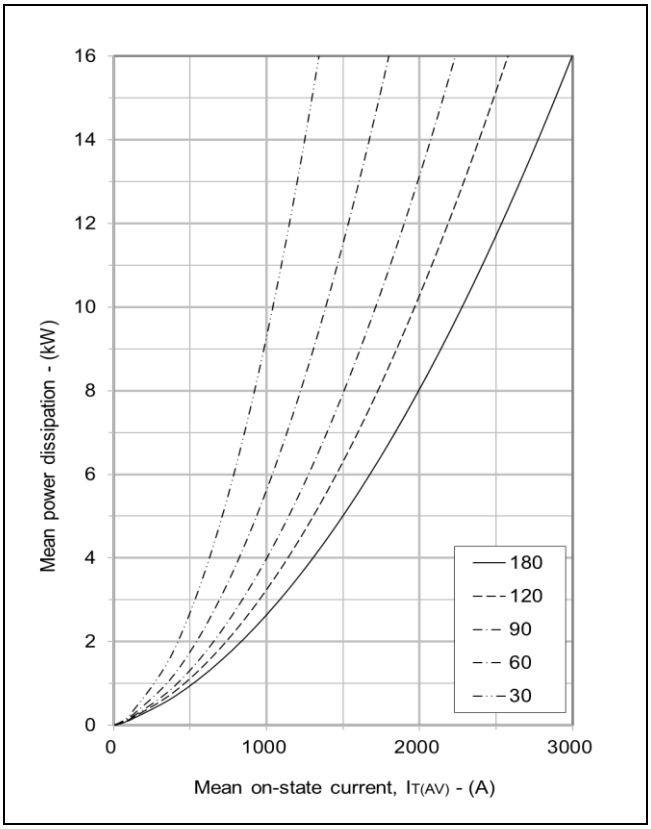



**Fig. 3 On-state power dissipation - sine wave**

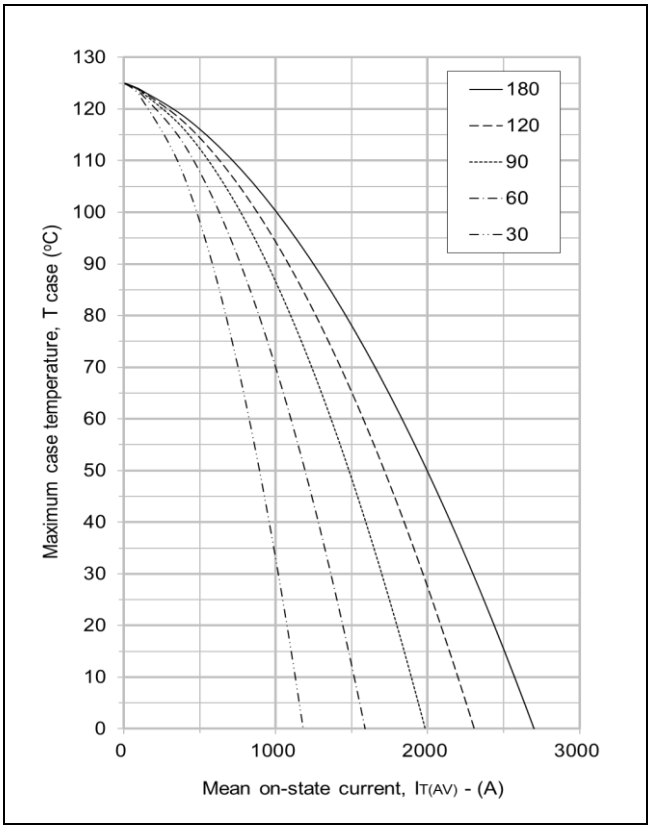



**Fig. 4 Maximum permissible case temperature, double side cooled - sine wave**

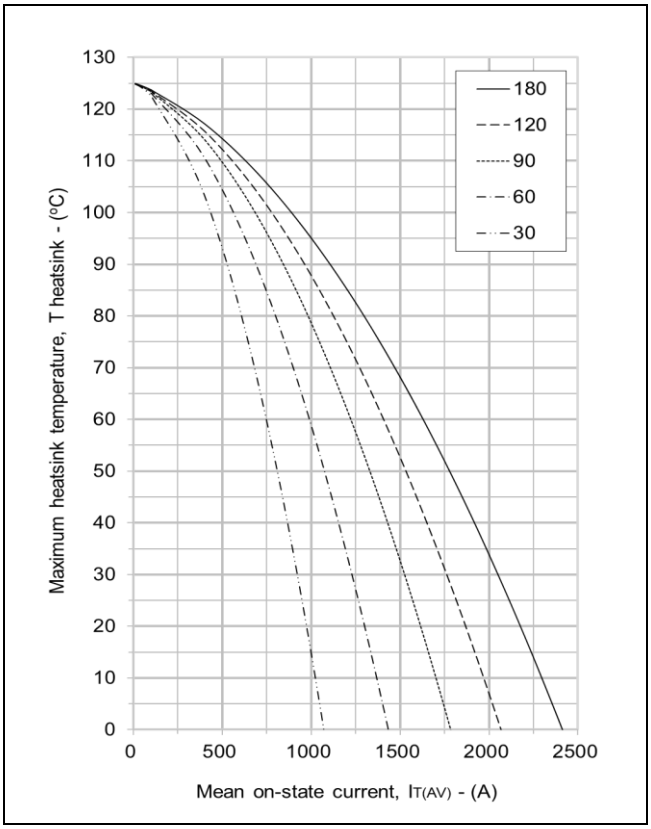



**Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave**

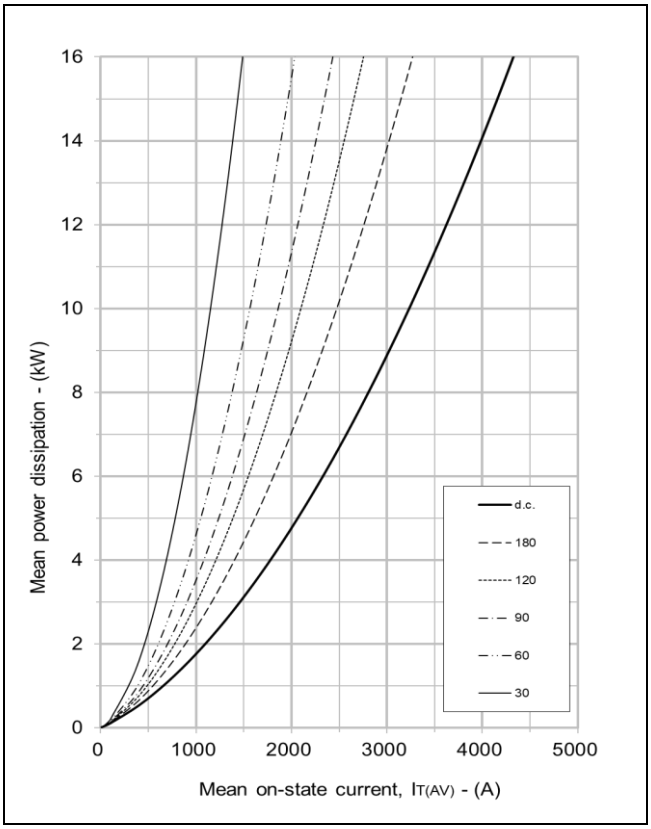



**Fig. 6 On-state power dissipation - rectangular wave**

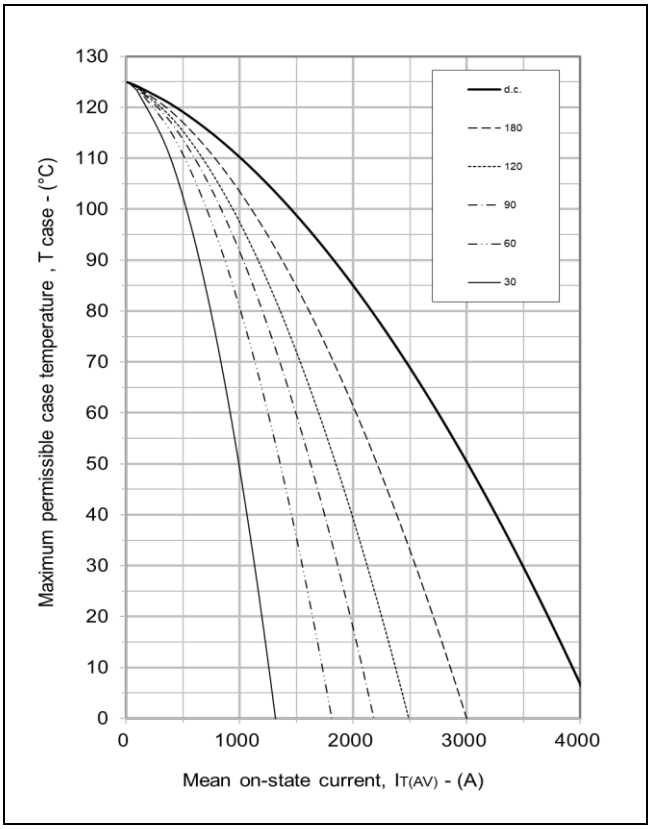



**Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave**

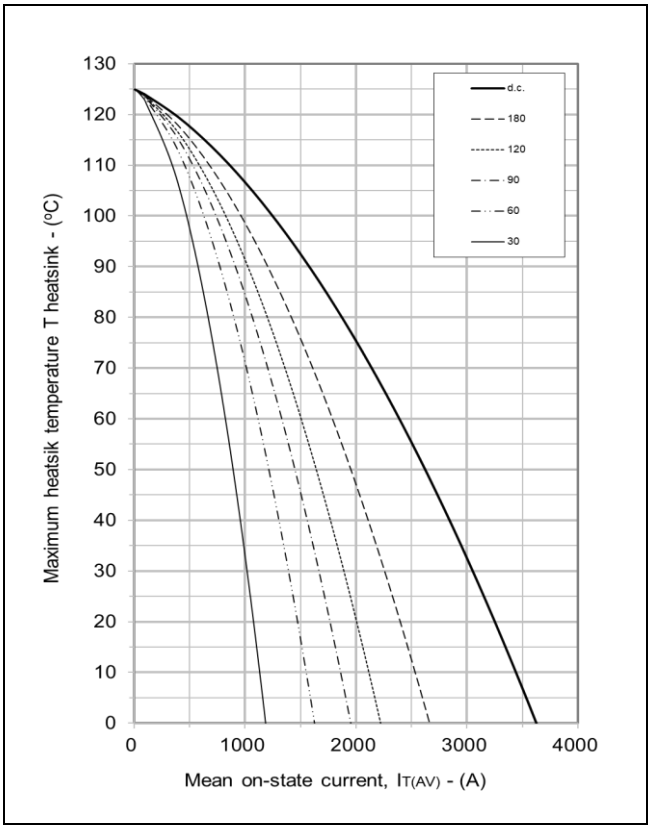
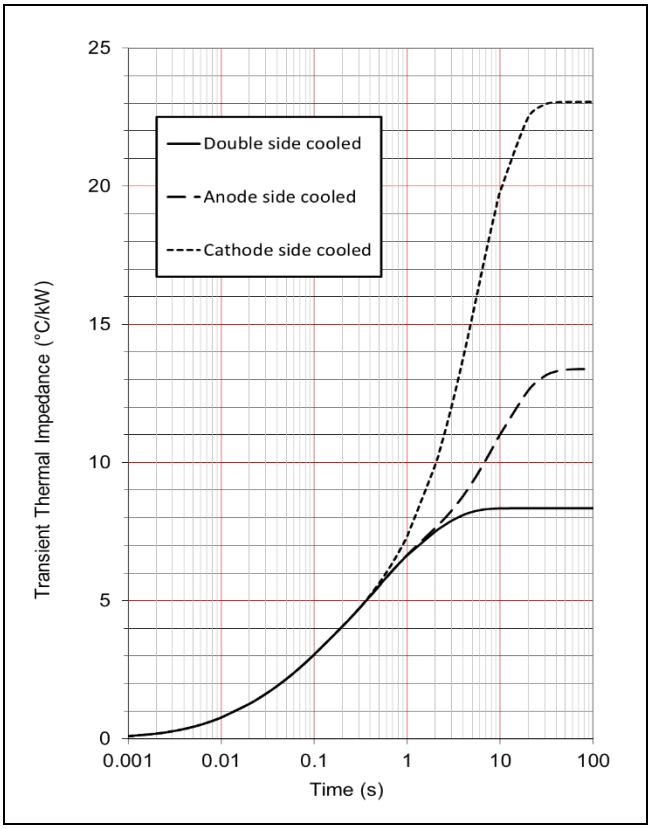



**Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave**




| | | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|
| Double side cooled | Ri(°C/kW) | 0.612 | 1.772 | 3.105 | 2.861 |
| | Ti(s) | 0.010 | 0.056 | 0.333 | 1.632 |
| Anode side cooled | Ri(°C/kW) | 0.701 | 1.939 | 3.610 | 7.138 |
| | Ti(s) | 0.011 | 0.066 | 0.420 | 9.061 |
| Cathode side cooled | Ri(°C/kW) | 0.673 | 2.017 | 1.731 | 18.639 |
| | Ti(s) | 0.011 | 0.066 | 0.304 | 5.727 |

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

| Double side cooling | | |
|---|---|---|
| | $\Delta Z_{th}$ (z) | |
| θ° | sine. | rect. |
| 180 | 0.94 | 0.65 |
| 120 | 1.09 | 0.92 |
| 90 | 1.24 | 1.07 |
| 60 | 1.38 | 1.23 |
| 30 | 1.49 | 1.40 |
| 15 | 1.54 | 1.49 |

| Anode Side Cooling | | |
|---|---|---|
| | $\Delta Z_{th}$ (z) | |
| θ° | sine. | rect. |
| 180 | 0.94 | 0.64 |
| 120 | 1.08 | 0.91 |
| 90 | 1.23 | 1.06 |
| 60 | 1.37 | 1.22 |
| 30 | 1.47 | 1.38 |
| 15 | 1.52 | 1.47 |

| Cathode Sided Cooling | | |
|---|---|---|
| | $\Delta Z_{th}$ (z) | |
| θ° | sine. | rect. |
| 180 | 0.94 | 0.64 |
| 120 | 1.08 | 0.91 |
| 90 | 1.24 | 1.06 |
| 60 | 1.37 | 1.22 |
| 30 | 1.48 | 1.39 |
| 15 | 1.53 | 1.48 |

**Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)**

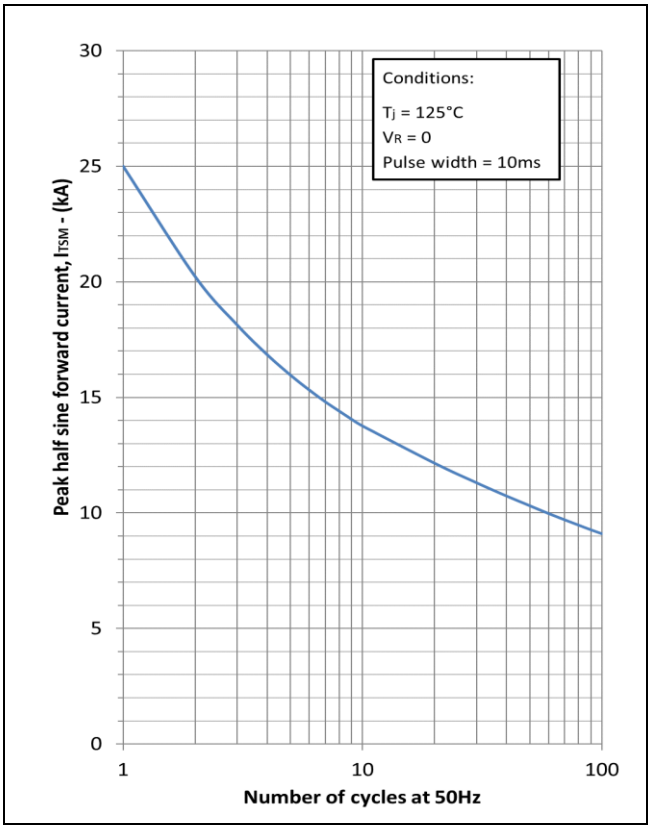



Fig. 10 Multi-cycle surge current

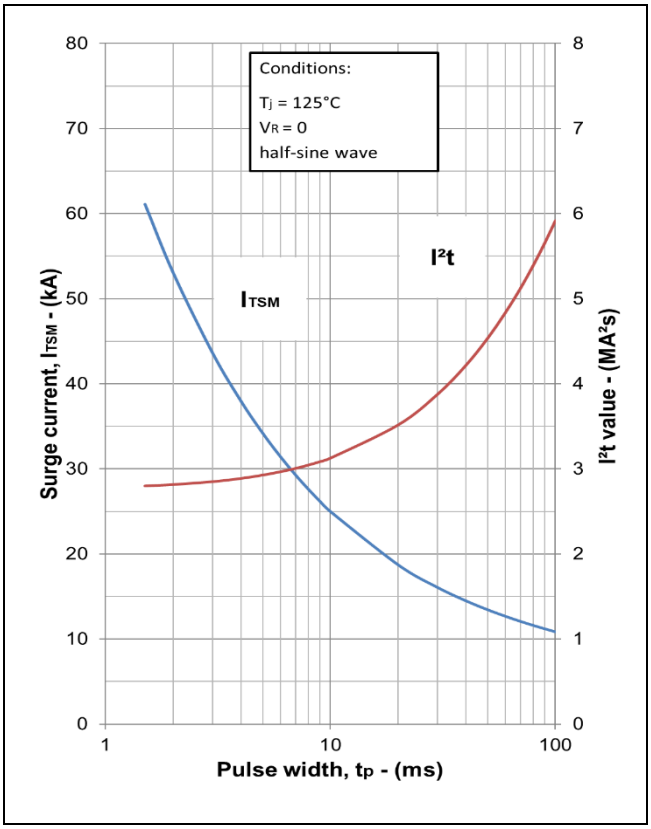



Fig. 11 Single-cycle surge current

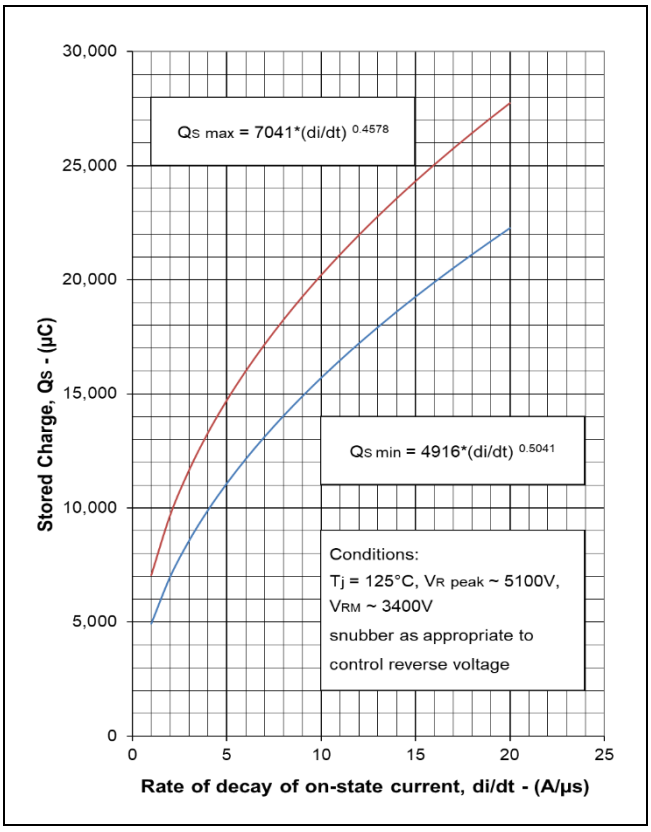



Fig. 12 Stored charge

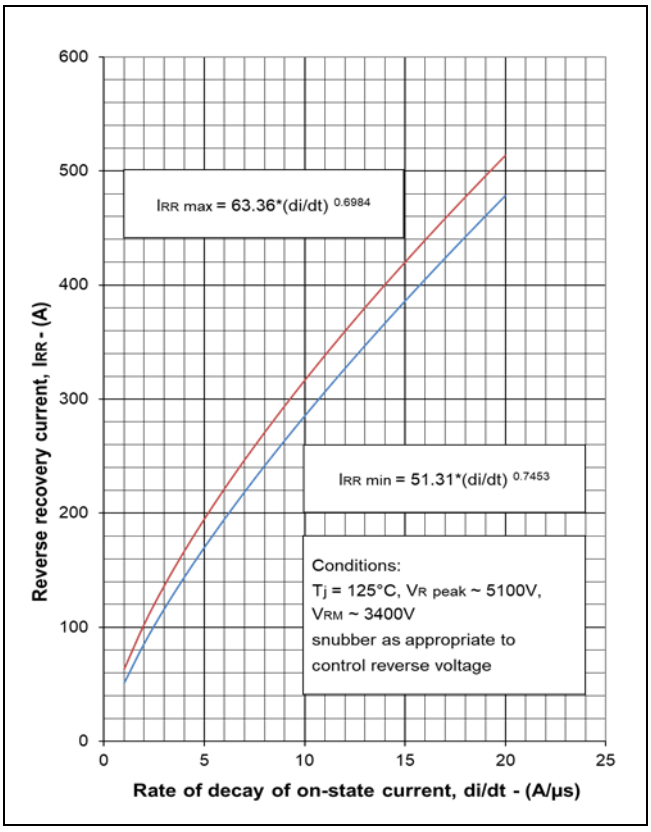



Fig. 13 Reverse recovery current

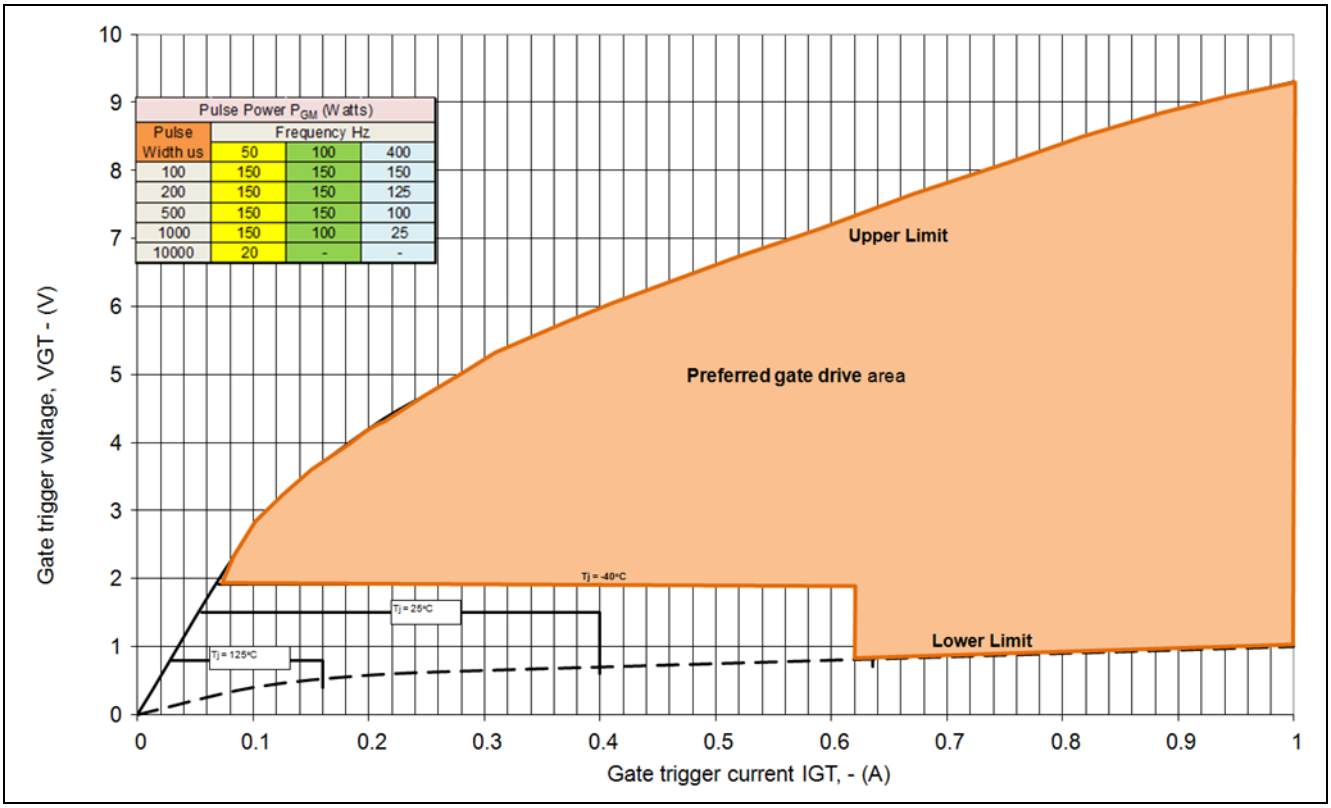



**Fig. 14 Gate characteristics**

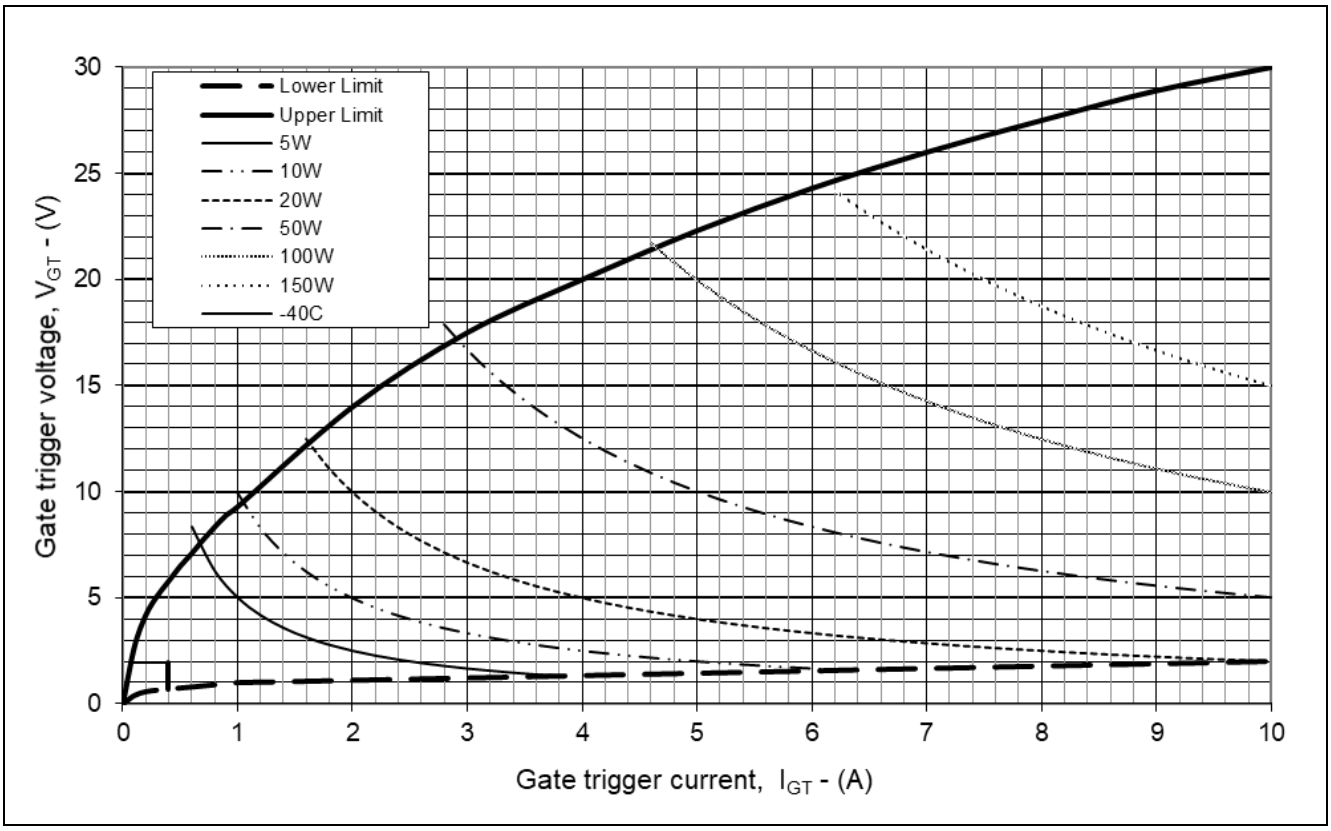


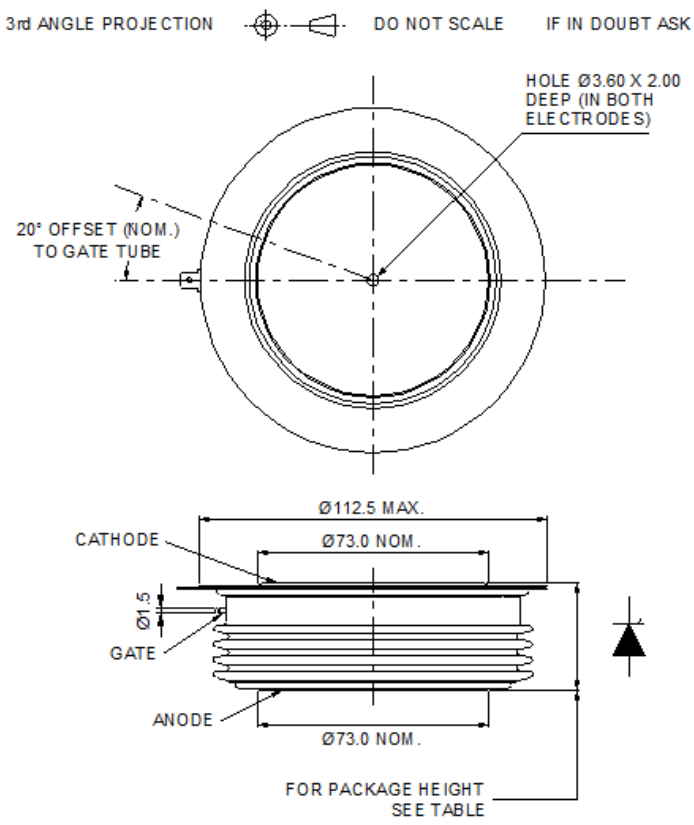

**Fig. 15 Gate characteristics**

## PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE




| Device | Maximum Thickness (mm) | Minimum Thickness (mm) |
|---|---|---|
| **DCR1840Y85** | 36.1 | 35.4 |
| DCR2220Y65 | 35.7 | 35.1 |
| DCR2630Y52 | 35.5 | 34.9 |
| DCR2930Y42 | 35.4 | 34.7 |
| DCR3650Y28 | **35.1** | **34.5** |
| DCR3910Y22 | 35.0 | 34.4 |
| DCR4740Y18 | 35.0 | 34.3 |

Lead length: 420mm

Lead terminal connector: M4 ring

**Package outline type code: Y**

**Fig. 16 Package outline**

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|---|---|
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