

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Bridge Rectifiers
- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR2560A85*	8500	$T_{vj} = -40^{\circ}\text{C}$ to 125°C ,
DCR2560A80	8000	$I_{DRM} = I_{RRM} = 300\text{mA}$,
DCR2560A75	7500	$V_{DRM}, V_{RRM} t_p = 10\text{ms}$
DCR2560A70	7000	$V_{DSM} \& V_{RSM} =$
		$V_{DRM} \& V_{RRM} + 100\text{V}$ respectively

Lower voltage grades available.

*8200V @ -40°C , 8500V @ 0°C

KEY PARAMETERS

V_{DRM}	8500V
$I_{T(AV)}$	2610A
I_{TSM}	34500A
dV/dt^*	1500V/μs
dI/dt	200A/μs

* Higher dV/dt selections are available on request

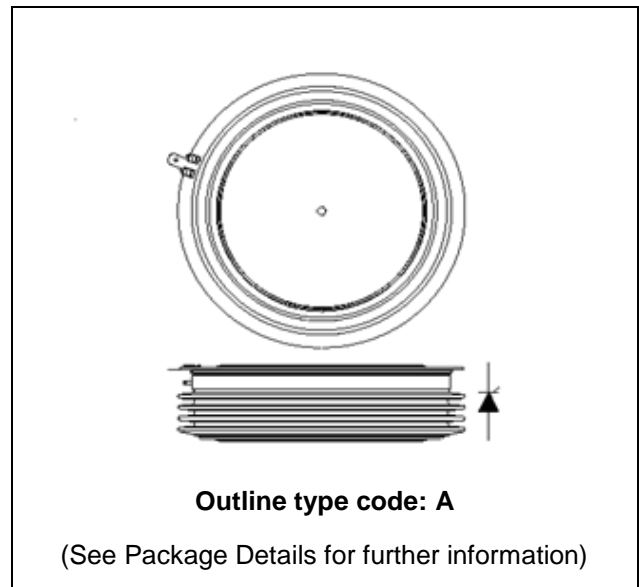


Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2560A85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2610	A
$I_{T(RMS)}$	RMS value	-	4100	A
I_r	Continuous (direct) on-state current	-	3790	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$ $V_R = 0$	34.5	kA
I^2t	I^2t for fusing		5.95	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	6.0	$^{\circ}\text{C}/\text{kW}$
		Single side cooled	Anode DC	-	10.4	$^{\circ}\text{C}/\text{kW}$
			Cathode DC	-	14.9	$^{\circ}\text{C}/\text{kW}$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 83kN (with mounting compound)	Double side	-	1.0	$^{\circ}\text{C}/\text{kW}$
			Single side	-	2.0	$^{\circ}\text{C}/\text{kW}$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$	
F_m	Clamping force		74	91	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	300	mA
		At 50% V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	30	-	mA

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
V_{TM}	Instantaneous forward voltage	At 4000A peak, $T_j = 125^{\circ}C$	2.65	2.95	V	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μ s	
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$ Gate source 30V, 10 Ω $t_r < 0.5\mu$ s, $T_j = 125^{\circ}C$	Repetitive 50Hz	-	100	A/ μ s
			Non-repetitive	-	200	A/ μ s
V_{T(ro)}	Threshold voltage - Low level	500A to 3200A at $T_{case} = 125^{\circ}C$	-	1.24	V	
	Threshold voltage - High level	3200A to 9000A at $T_{case} = 125^{\circ}C$	-	1.43	V	
r_T	On-state slope resistance - Low level	500A to 3200A at $T_{case} = 125^{\circ}C$	-	0.44	m Ω	
	On-state slope resistance - High level	3200A to 9000A at $T_{case} = 125^{\circ}C$	-	0.38	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu$ s, $T_j = 25^{\circ}C$	-	3	μ s	
t_q	Turn-off time	$I_T = 3000A$, $T_j = 125^{\circ}C$, $V_R = 200V$, $dI/dt = 1A/\mu$ s, $dV_{DR}/dt = 20V/\mu$ s linear	-	1000	μ s	
Q_s	Stored charge	$I_T = 2000A$, $T_j = 125^{\circ}C$, $dI/dt = 1A/\mu$ s	5150	7240	μ C	
I_{RR}	Reverse recovery current	$V_R \sim 3400V$, $C_s = 1.5\mu$ F, $R_s = 63\Omega$	57	68	A	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	0.4	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	400	mA
I_{GD}	Gate non-trigger current	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	10	mA

CURVES

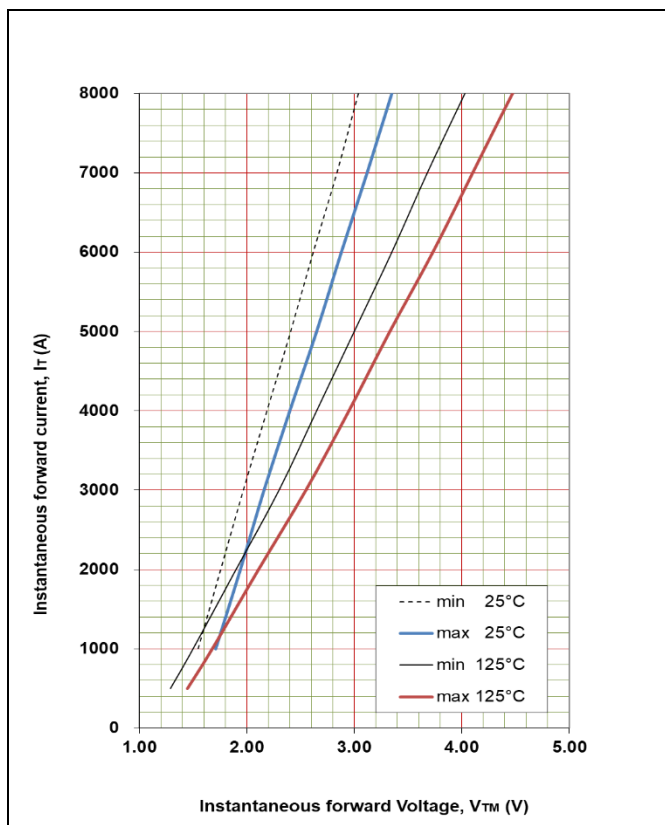


Fig. 2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where $A = -0.047872$

$B = 0.229354$

$C = 0.000394$

$D = -0.007695$

These values are valid for $T_j = 125^{\circ}C$ for I_T 500A to 9000A

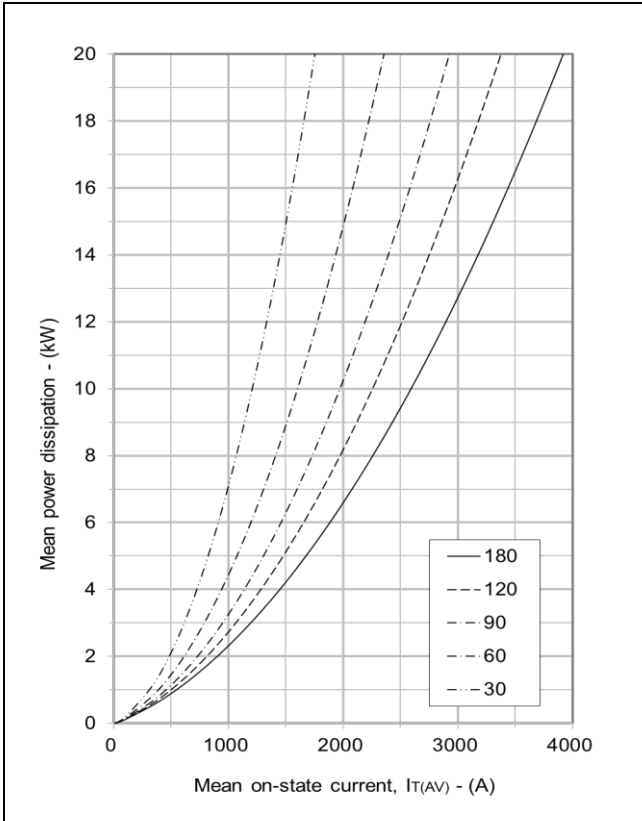


Fig. 3 On-state power dissipation - sine wave

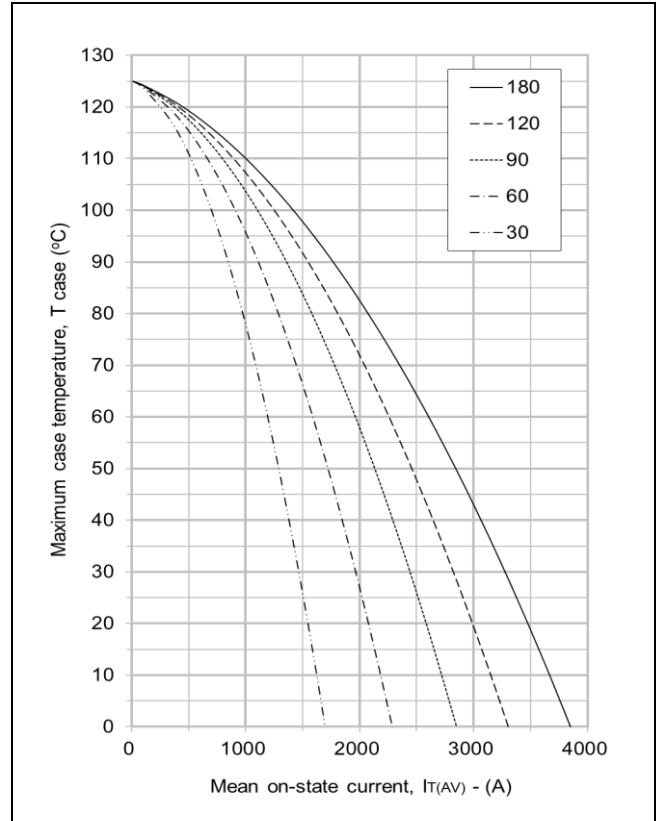


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

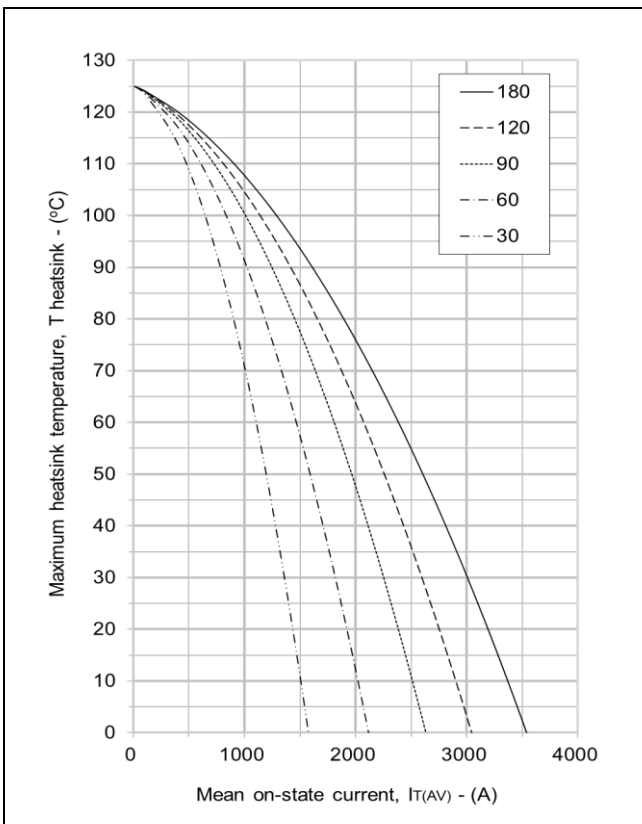


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

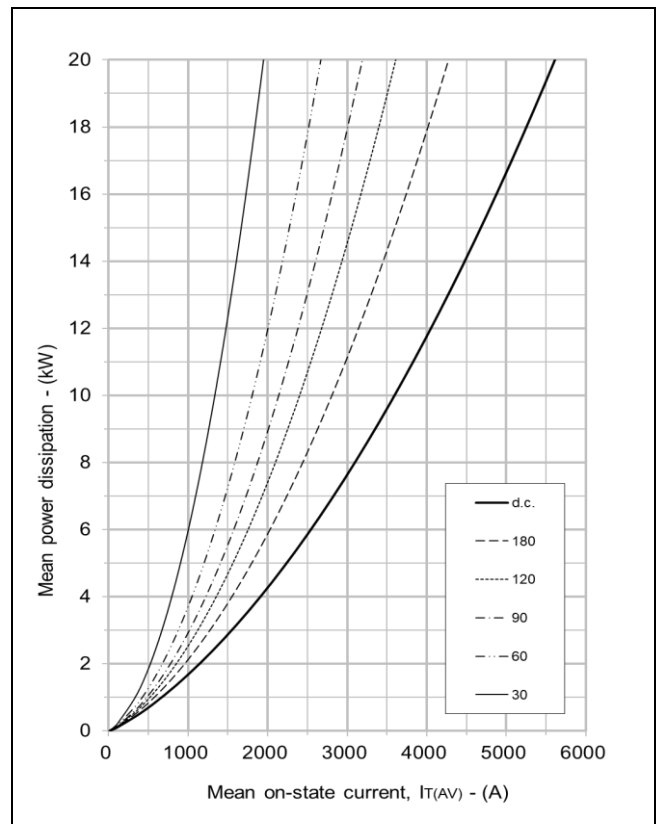


Fig. 6 On-state power dissipation - rectangular wave

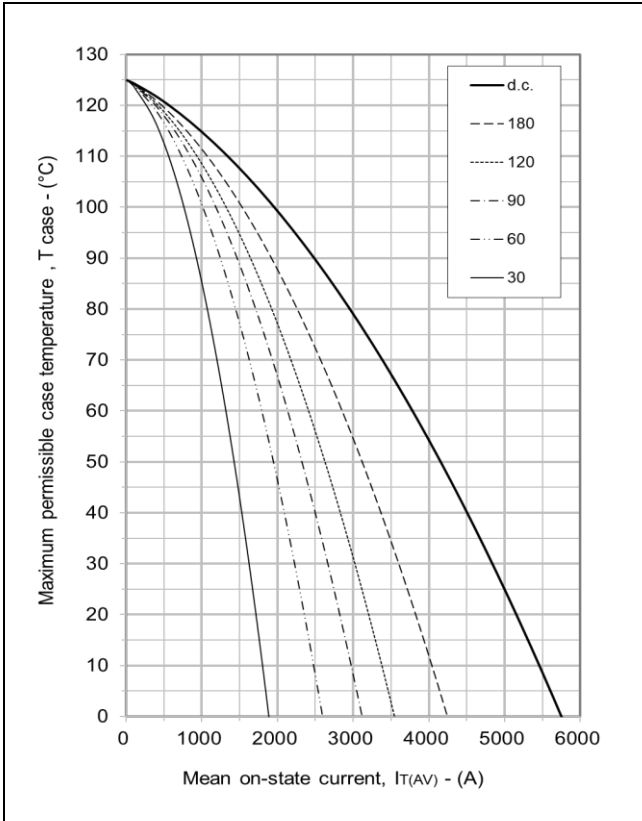


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

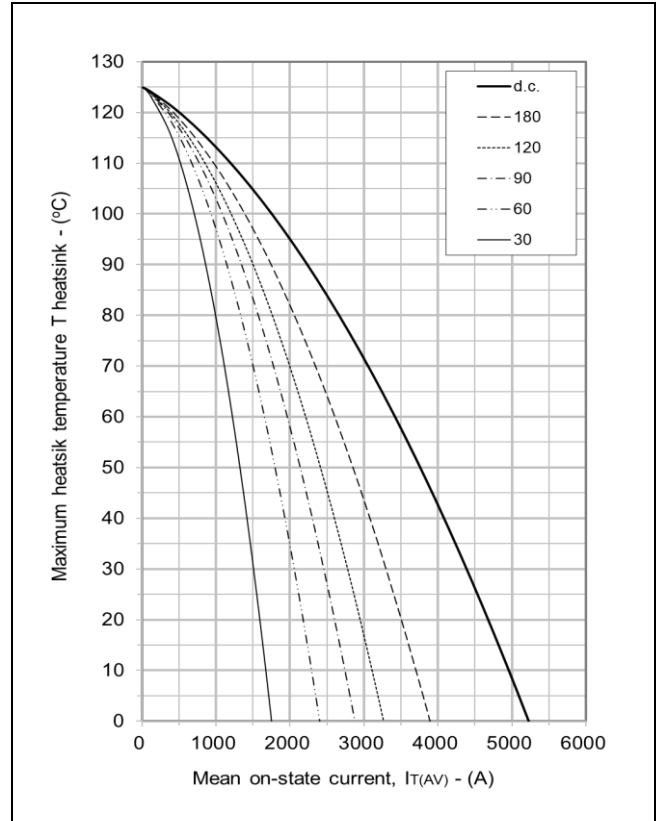


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

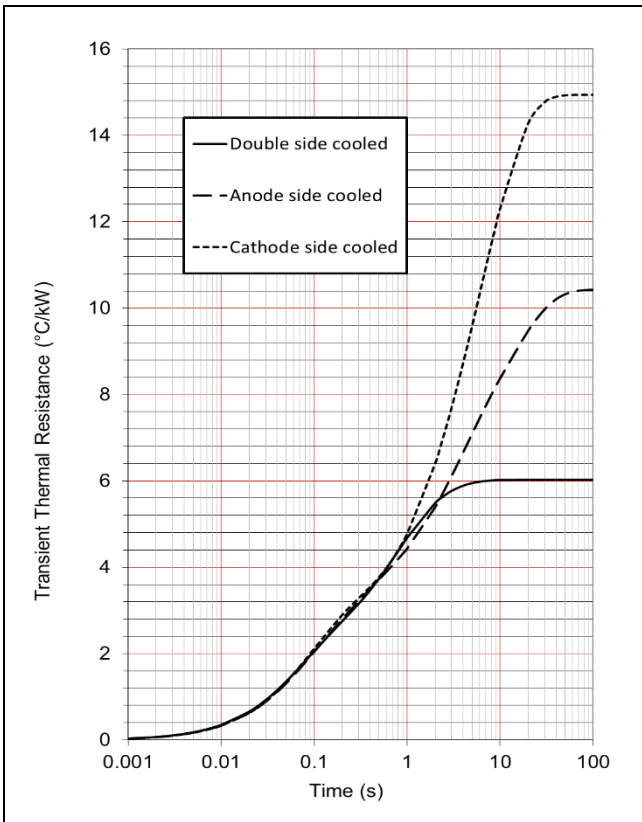


Fig.9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

		1	2	3	4
Double side cooled	Ri(°C/kW)	3.015	1.049	0.984	0.984
	Ti(s)	0.704	1.905	0.059	0.059
Anode side cooled	Ri(°C/kW)	3.156	4.093	1.557	1.624
	Ti(s)	2.690	13.792	0.059	0.206
Cathode side cooled	Ri(°C/kW)	7.077	3.483	1.746	2.634
	Ti(s)	6.649	8.436	1.762	0.081

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
θ°	$\Delta Z_{th} (z)$		θ°	$\Delta Z_{th} (z)$		θ°	$\Delta Z_{th} (z)$	
	sine.	rect.		sine.	rect.		sine.	rect.
180	0.44	0.31	180	0.42	0.30	180	0.42	0.30
120	0.49	0.43	120	0.47	0.41	120	0.47	0.41
90	0.55	0.49	90	0.52	0.46	90	0.52	0.46
60	0.60	0.55	60	0.57	0.52	60	0.57	0.52
30	0.64	0.61	30	0.61	0.58	30	0.60	0.58
15	0.66	0.64	15	0.62	0.61	15	0.62	0.60

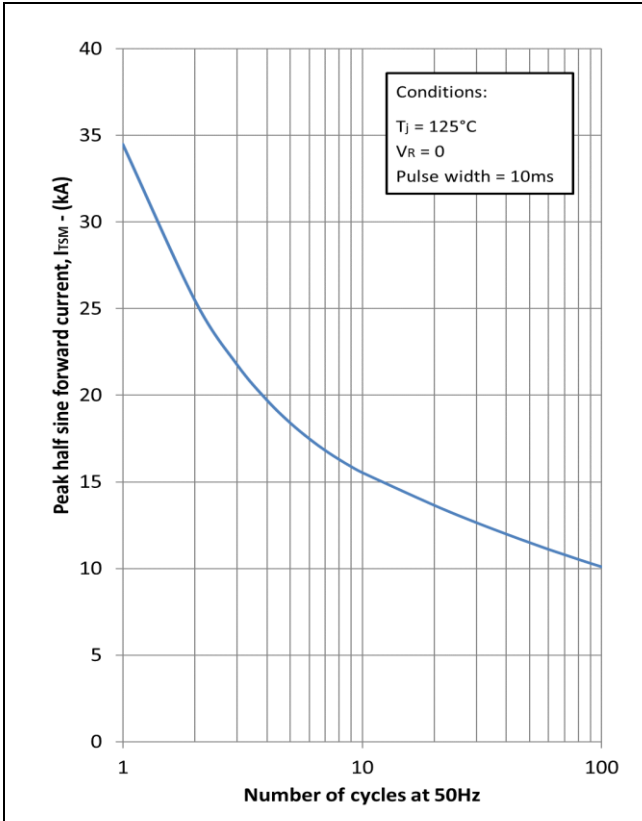


Fig. 10 Multi-cycle surge current

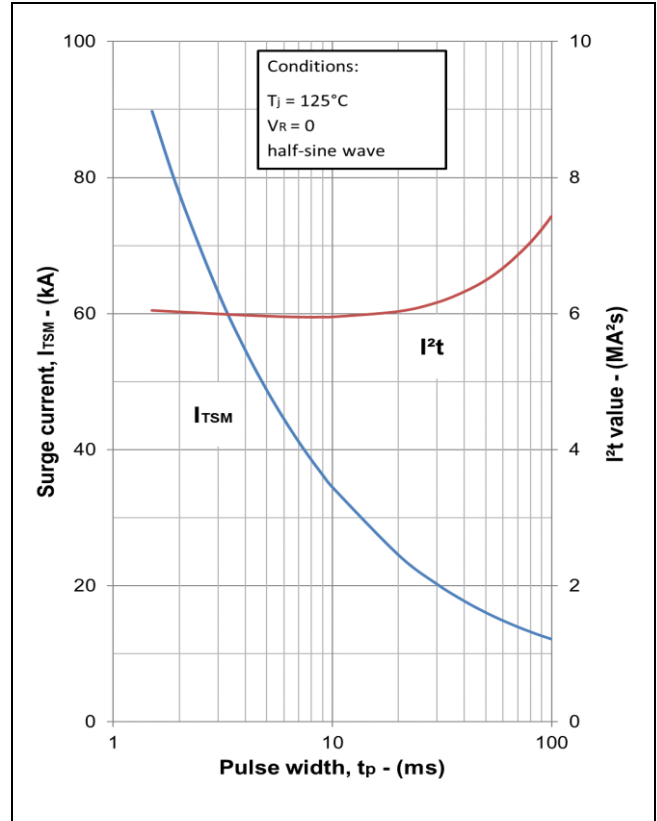


Fig. 11 Single-cycle surge current

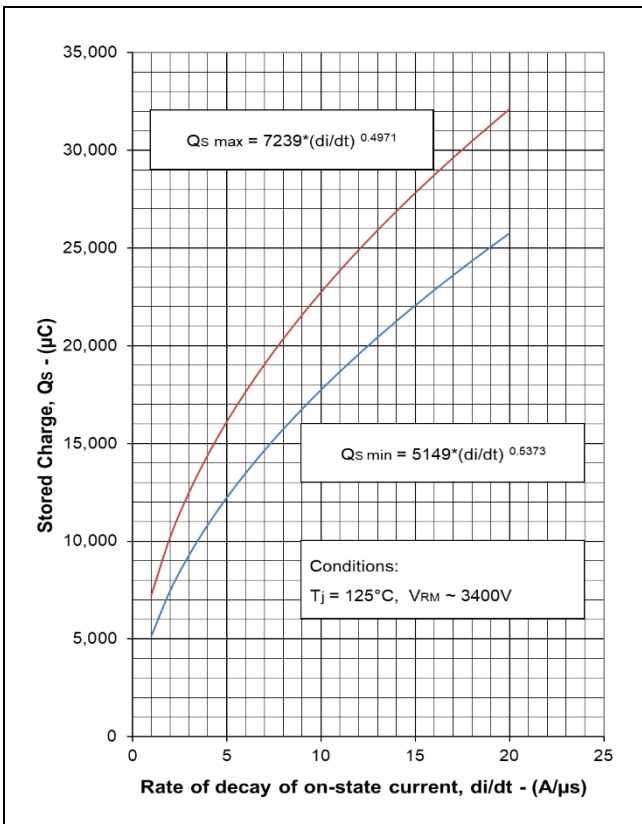


Fig. 12 Stored charge

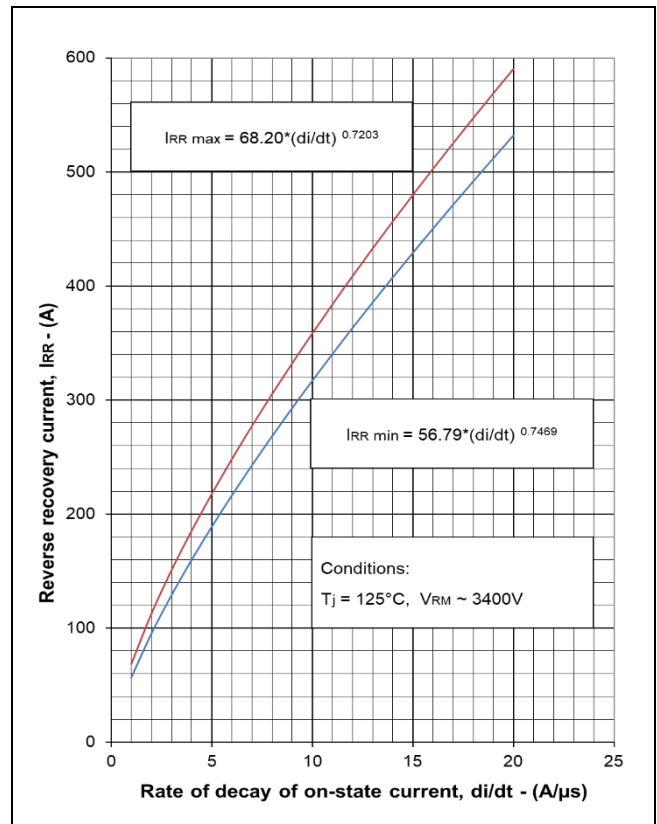


Fig. 13 Reverse recovery current

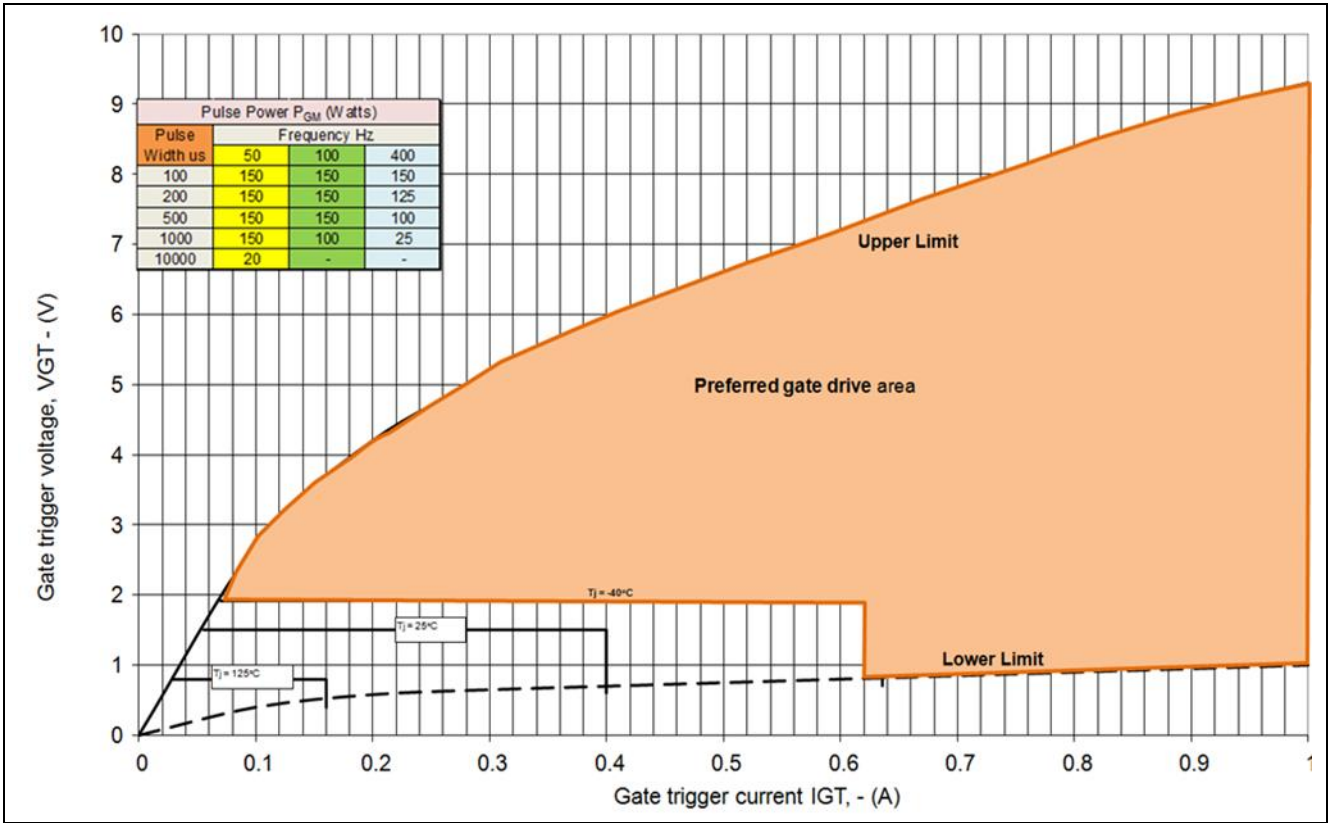


Fig.14 Gate characteristics

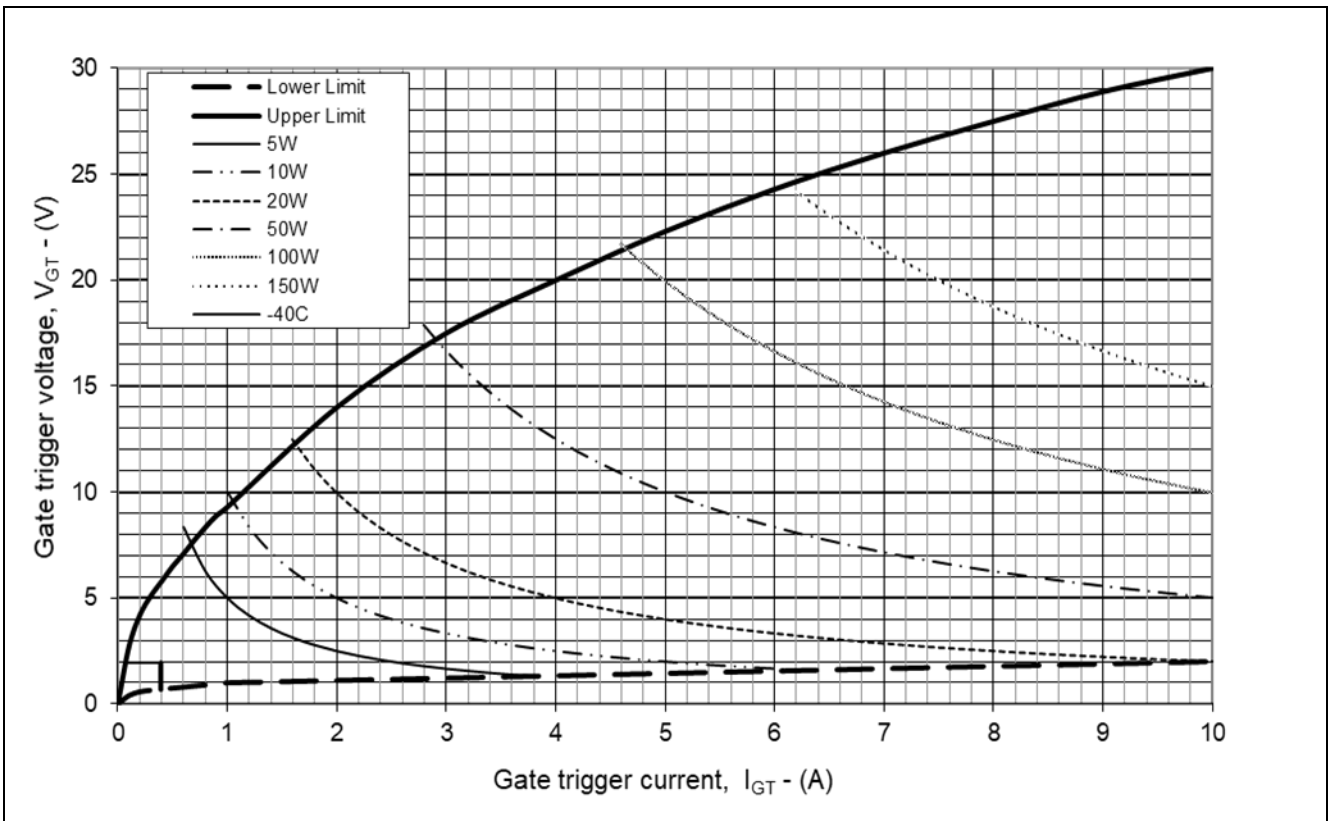


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

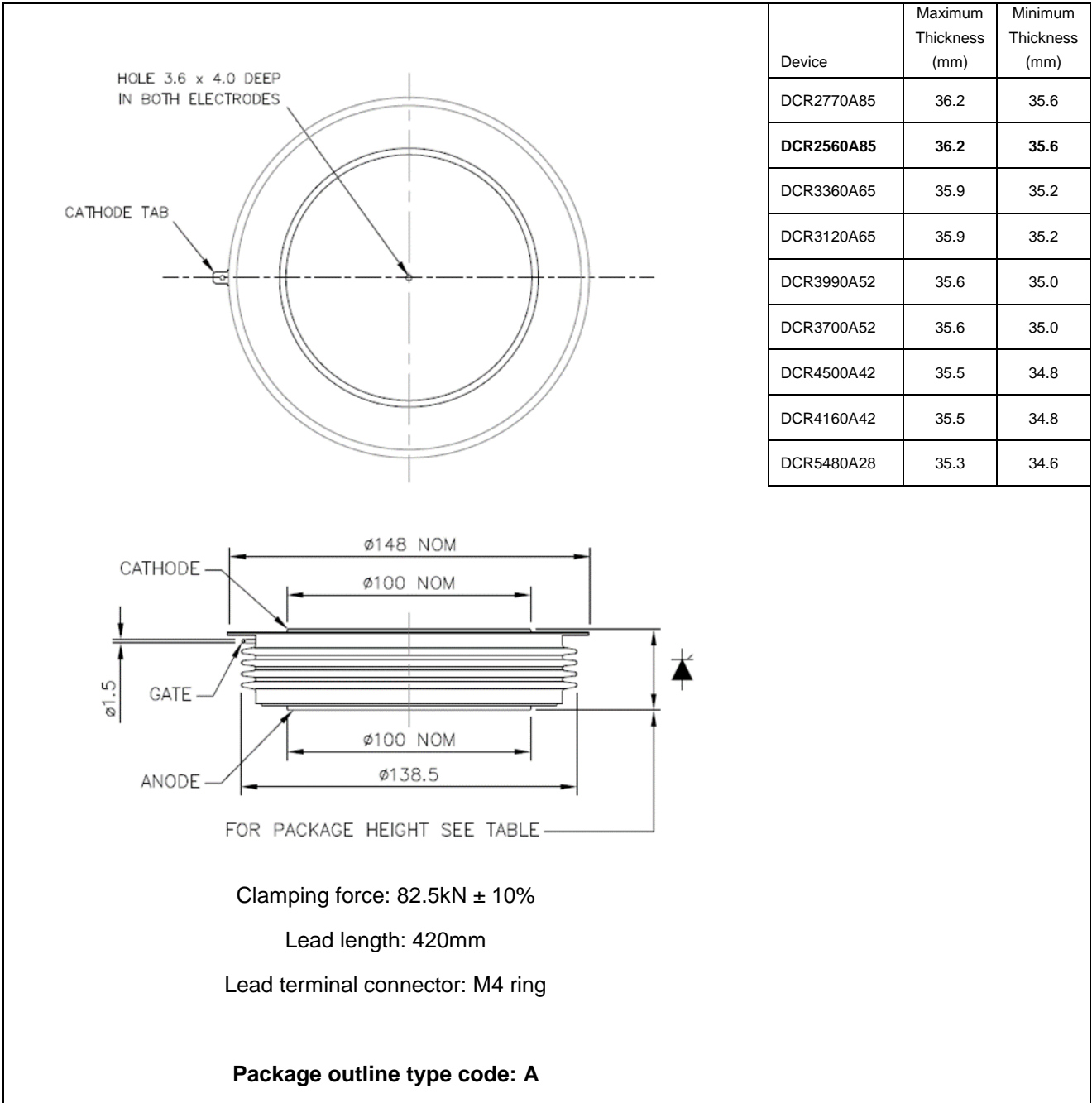


Fig. 16 Package outline

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