DCR720E18

Phase Control Thyristor

Replaces DS6025-2 DS6025-3 July 2020 (LN40091)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

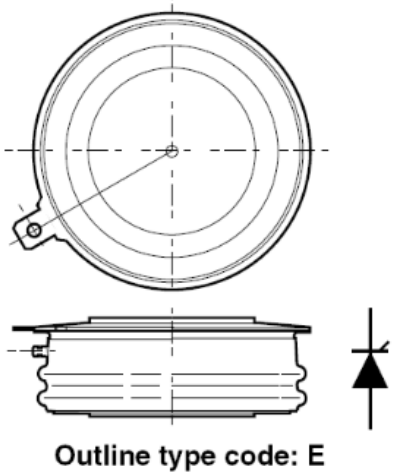
V_{DRM}	**1800V**
$I_{T(AV)}$	**720A**
I_{TSM}	**8300A**
dV/dt*	**1000V/µs**
dI/dt	**200A/µs**

*** Higher dV/dt selections are available**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR720E18 DCR720E16 DCR720E14 DCR720E12	1800 1600 1400 1200	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 30mA, V_{DRM}, V_{RRM} t_p = 10ms V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.



(See Package Details for further information)

Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR720E18

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	720	A
$I_{T(RMS)}$	RMS value	-	1230	A
I_T	Continuous (direct) on-state current	-	970	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	8.3	kA
I^2t	I^2t for fusing	V_R = 0	0.344	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	0.041	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Double side cooled	DC	-	0.01	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-40	140	°C
F_m	Clamping force			4	6	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	30	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1000A Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Repetitive	-	200	A/µs
			Non-repetitive	-	1000	A/µs
V_T	On-state voltage	I_T = 1500A, T_{case} = 125°C			1.97	V
$V_{T(TO)}$	Threshold voltage	T_{case} = 125°C		-	1.09	V
r_T	On-state slope resistance	T_{case} = 125°C		-	0.587	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	T_j = 125°C, V_R = 100V, dI/dt = 10A/µs, dV_{DR}/dt = 20V/µs linear to 67% V_{DRM}		-	150	µs
Q_S	Stored charge	I_T = 1000A, T_j = 125°C, dI/dt = 10A/µs, t_p = 1000µs		-	1500	µC
I_{RR}	Reverse recovery current			-	110	A
I_L	Latching current	T_j = 25°C		-	1	A
I_H	Holding current	T_j = 25°C		-	200	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	3	V
V_{GD}	Gate non-trigger voltage	At 40% V_{DRM}, T_{case} = 125°C	0.3	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	300	mA
I_{GD}	Gate non-trigger current	At 40% V_{DRM}, T_{case} = 125°C	20	mA

CURVES

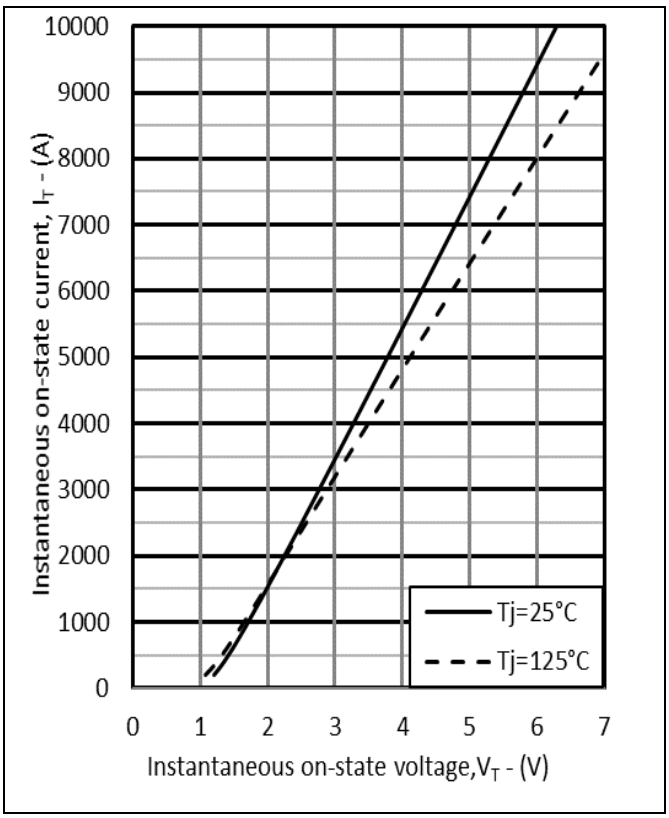


Fig. 2 Maximum on state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

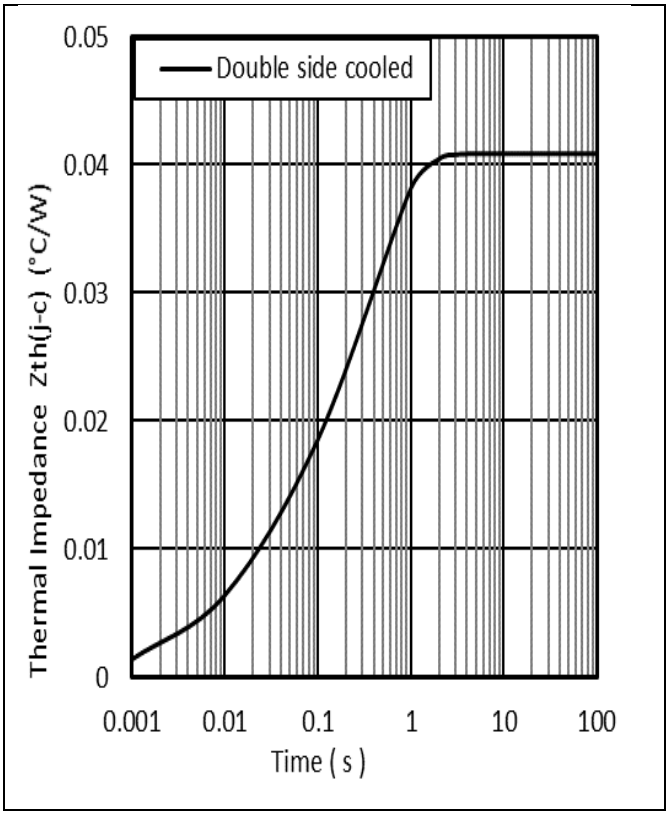
Where A = 0.213846

B = 0.177258

C = 0.000692251

D = -0.0152068

These values are valid for Tj = 125°C



$$R_{thjc}(t) = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	τ_i (s)	R_{thi} (°C/kW)
1	0.5391689	16.5
2	0.1940576	14.19235
3	0.0219527	7.412673
4	0.0021962	2.759765

Fig. 3 Maximum (limit) transient thermal impedance - junction to case (°C/W)

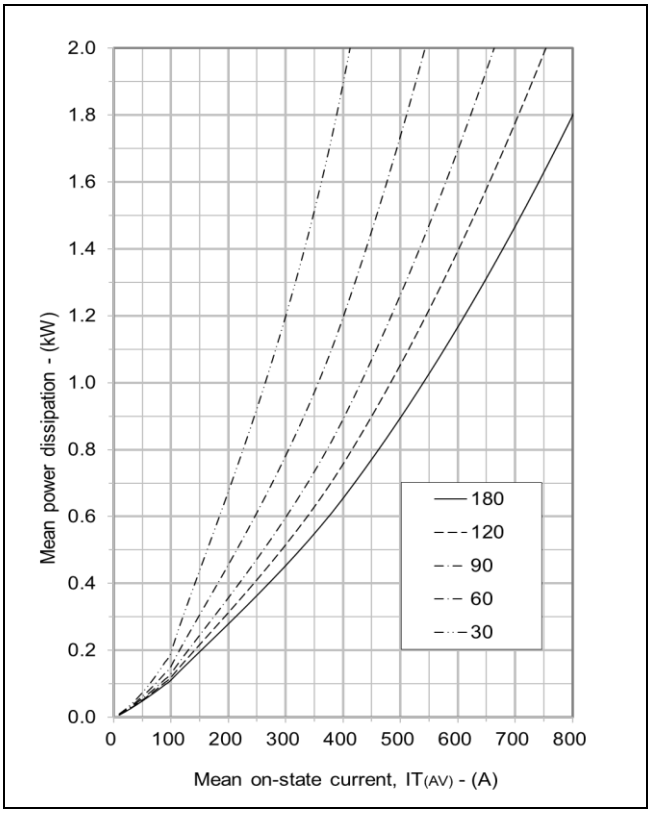


Fig. 4 On-state power dissipation - sine wave

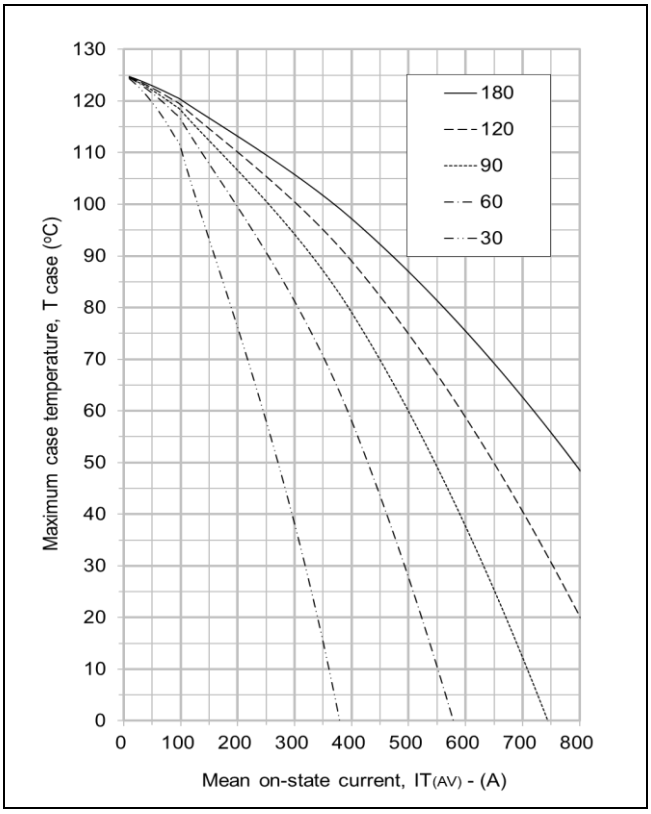


Fig. 5 Maximum permissible case temperature, double side cooled - sine wave

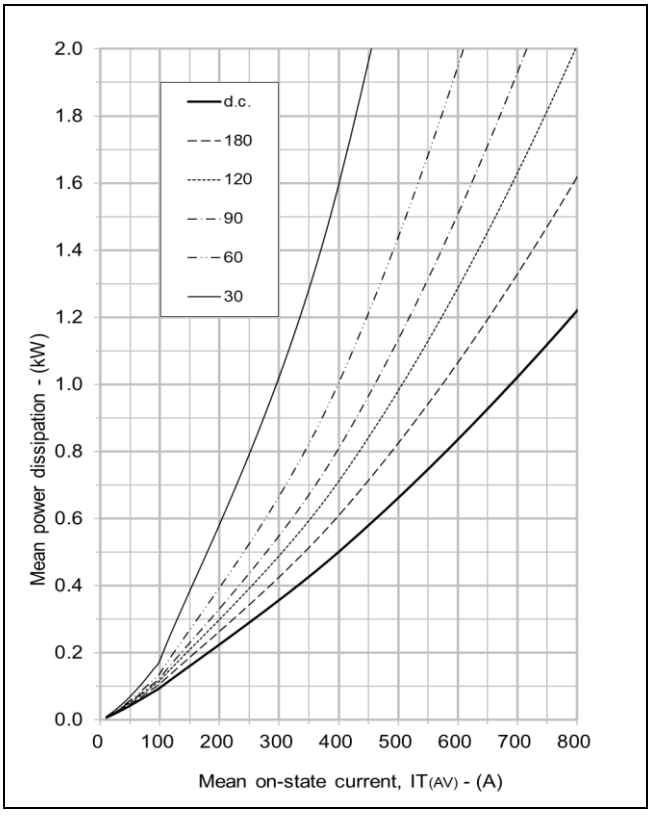


Fig. 6 On-state power dissipation - rectangular wave

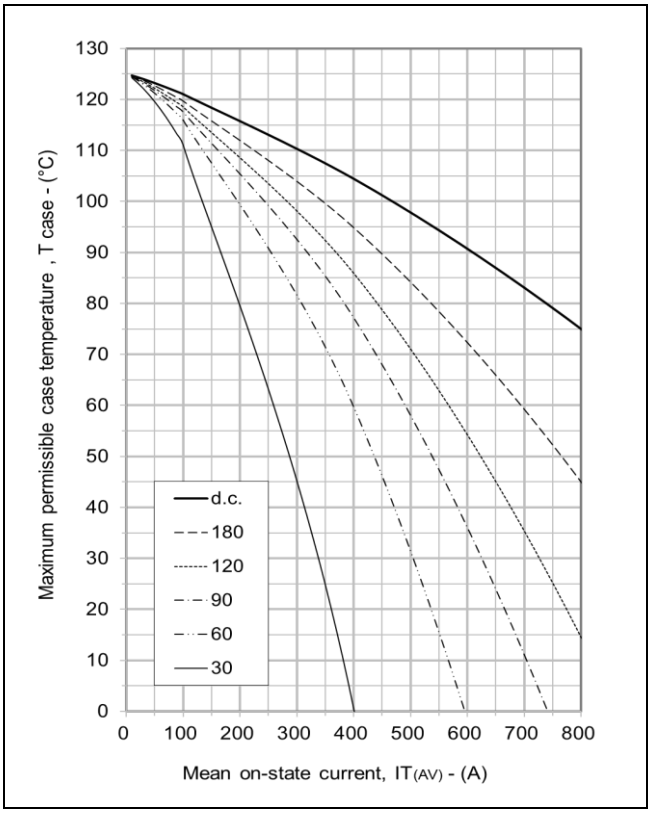


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

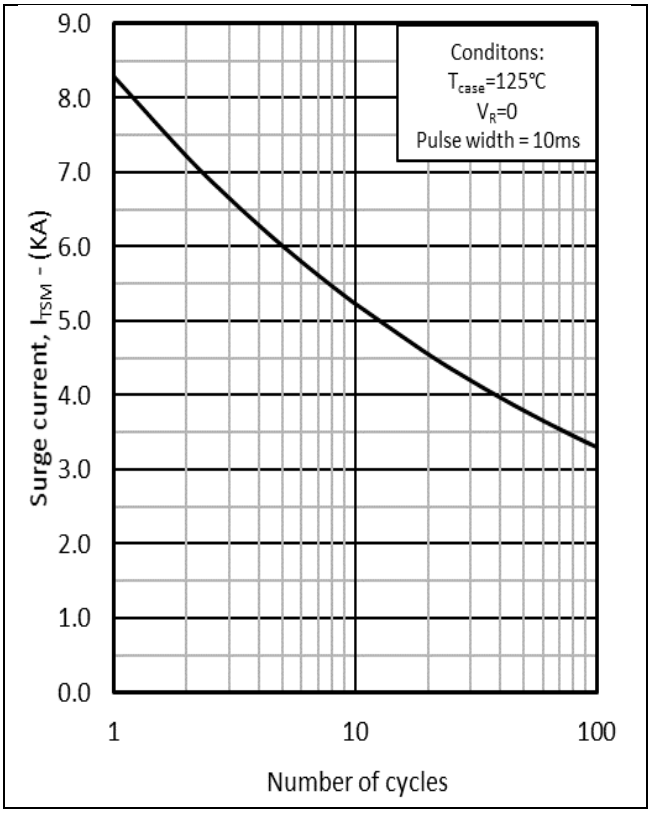


Fig. 8 Multi-cycle surge current

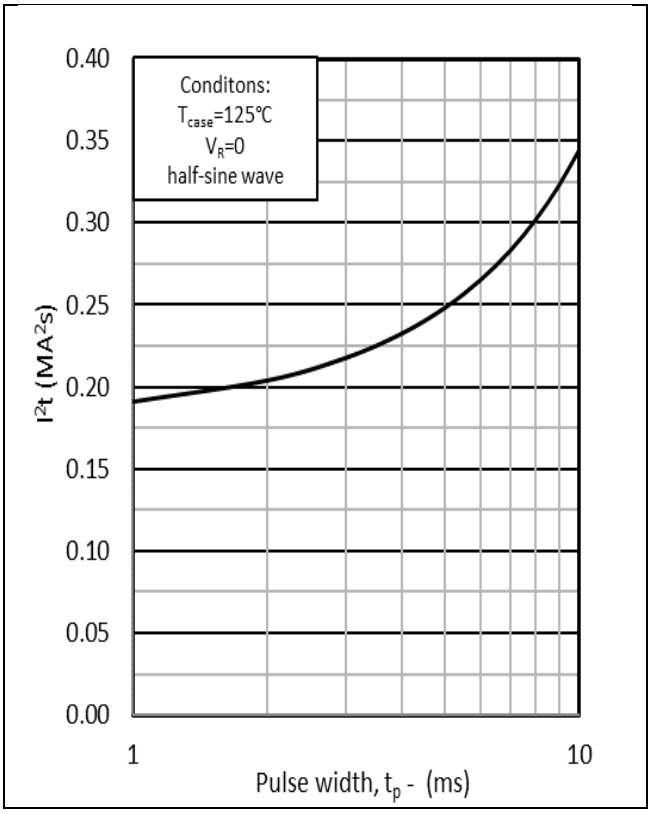


Fig. 9 Single-cycle I^2t

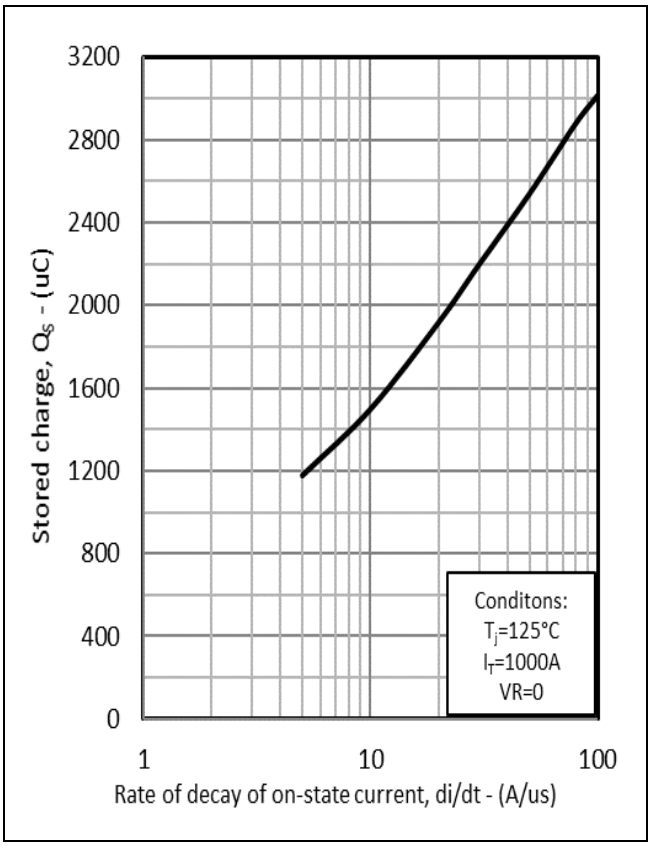


Fig. 10 Reverse recovery charge

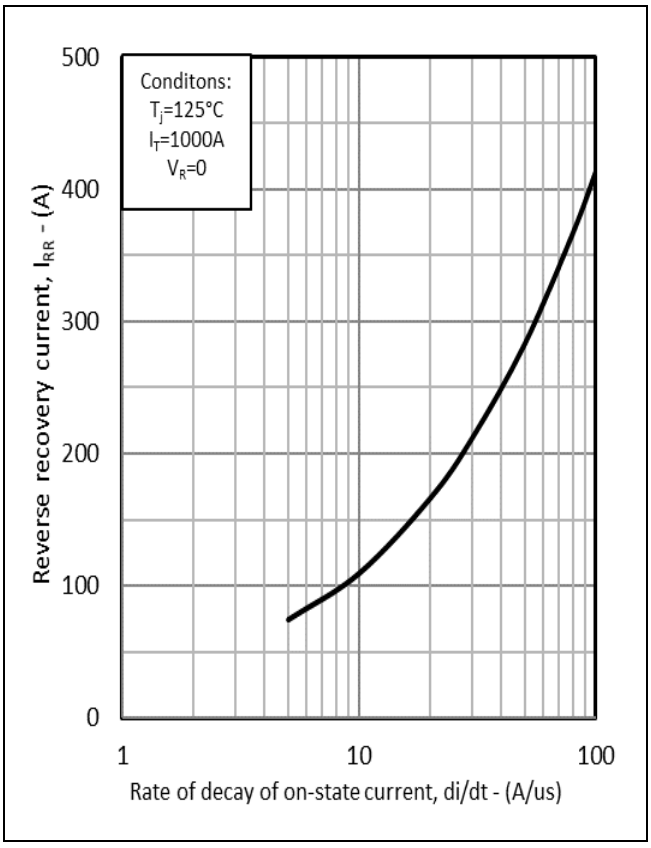


Fig. 11 Reverse recovery current

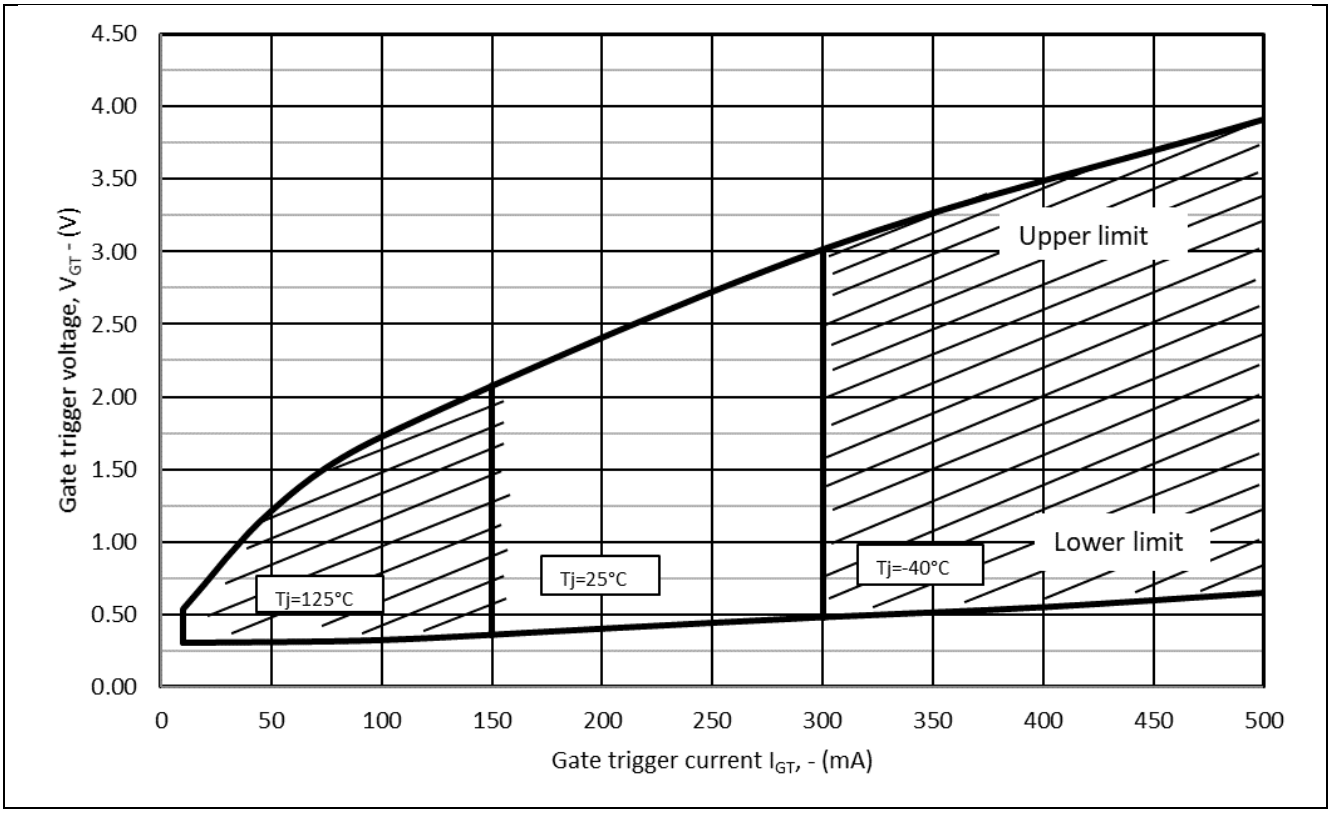
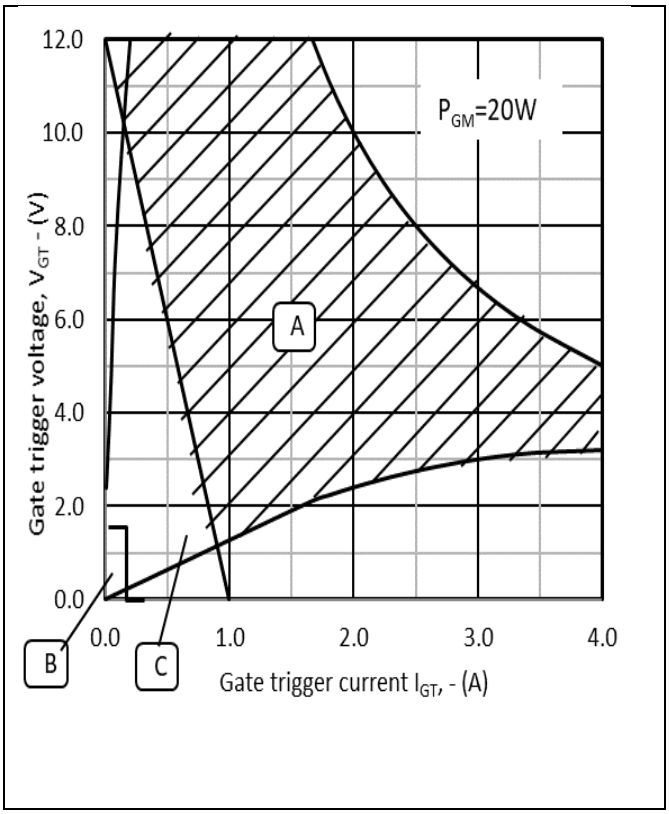


Fig. 12 Gate characteristics



A: is Recommended Triggering Area.

B: is Unreliable Triggering Area.

C: is Recommended Gate Load Line.

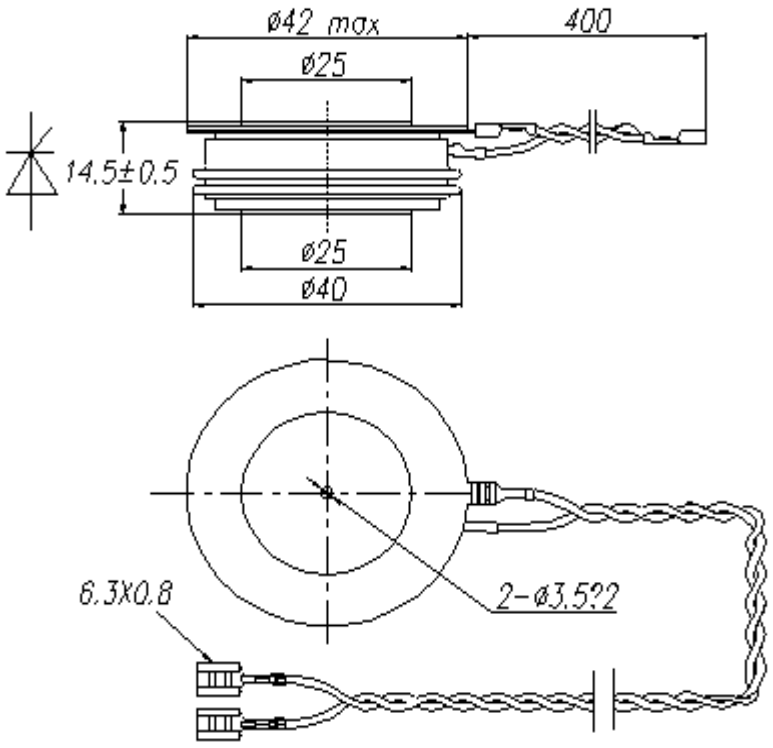
Fig. 13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Package outline type code: E

Fig. 14 Package outline

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